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APRIL 2013
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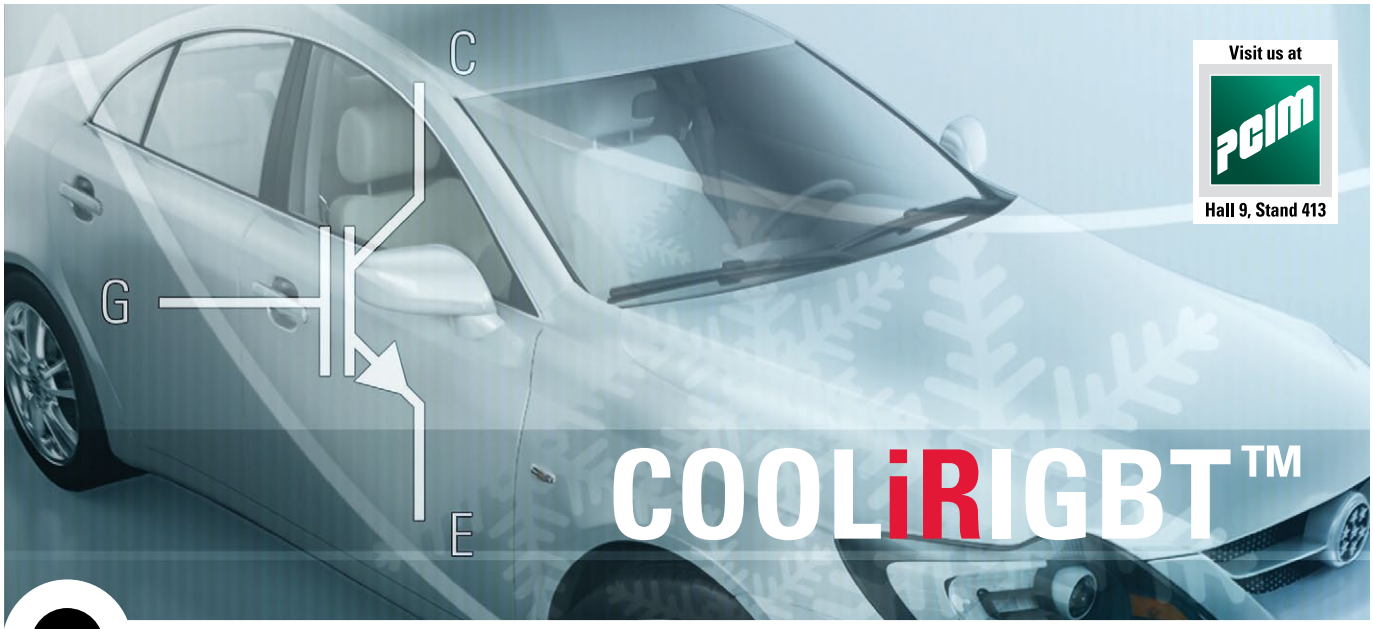

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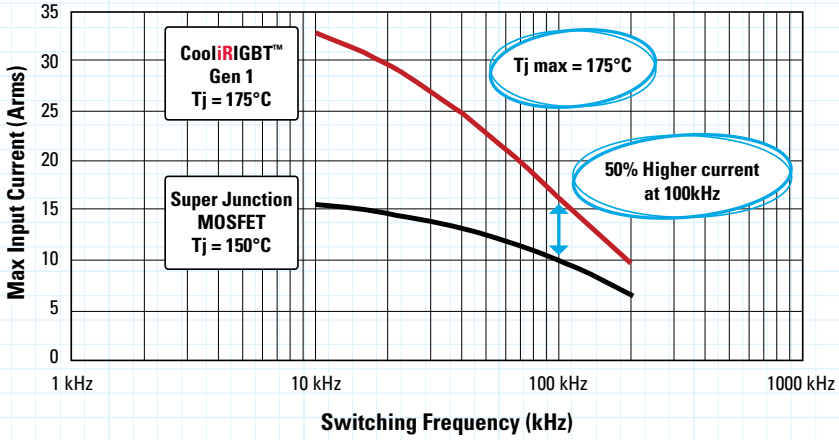

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VAT Registration: BE 461.357.437
RPM: Brussels
Company Number: 0461357437

EDN-EUROPE is published 11 times in 2013 by European Business Press SA,
7 Avenue Reine Astrid, 1310 La Hulpe, Belgium
Tel: +32-2-740 00 50 Fax: +32-2-740 00 59
email: info@eetimes.be. VAT Registration: BE 461.357.437.
RPM: Nivelles. Volume 15, Issue 2 EE Times P 304128
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More slices of the Pi

A smaller version of the Raspberry Pi computer built in the United Kingdom is driving the cost to less than $25; the world of “the Pi” continues to grow with new expansion modules and applications, and the platform continues to be promoted as the means of enticing young engineers into coding.

I am still sceptical – I have said this before in this column, but I’ll say it again – of the “moral panic” that has been constructed around the educational purposes of the Raspberry Pi. The contention is that we are not educating or training (there’s an important difference) enough software engineers who can code tomorrow’s applications: so, let’s give the kids a super-cheap but capable platform to play with and encourage them to get coding. Most times, whenever there is declared to be such a skills shortage, one of two explanations applies. Either simple supply-and-demand is at work and the respective industry has not been paying enough to attract new entrants: or, the industry is actively trying to manage the supply side of the equation so that it can pay less in the future and reduce its cost base.

In this case, though, my suggestion is that something deeper is at work. The Raspberry Pi phenomenon throws into sharp relief the abject failure, over 40-plus years, of at least one branch of computer science. The part of the subject dealing with languages and compilers could be said to aspire to enabling us to instruct computers what to do, in as close to our natural language as possible. Of course, between a command spoken in any human language and the extraction and expression of precise intention there are many subtle layers of meaning and interpretation. But in 50 years we have moved forward hardly at all.

The young coders we are trying to impress will likely work in Python; for sure, Python has a lot of work “under the hood” (implicit typing and all that, for example) that does help – but no user tapping Basic into a Sinclair Spectrum would need more than a few minutes to get the measure of it. For most professional work, we have nothing better than C: essentially warmed-over Algol, a language half a century old.

Surely in the 21st Century we should have only a very few exotic coders working at the level of typing indents and curly brackets and hash marks, and worrying about their type declarations and overflows. They should be the lowest layer in a hierarchy that enables us to tell computer hardware what to do in something a lot closer to natural language. The young product innovators we want to encourage should be able to express their intentions freely, without constant recourse to characters only reached by the Shift key. Instead, we have none of that: in that half-century we have progressed not at all. Once again, (at least) two possible explanations offer themselves.

The first is that this objective is in fact impossible; that navigating through the layers of subtlety of human language is far too complex a task for the sort of instructions we are discussing here, and we have no alternative to taking our brains down to the level of the hardware, and continuing to tell it what to do at not much more than bit-by-bit level. The second possibility is that computer scientists – and the people who make good coders – are in fact perfectly happy to appear a race apart, as exotic creatures who can handle the curly brackets and hash marks, a comprehension that is not given to the rest of us. Maybe, they just don’t want to evolve.

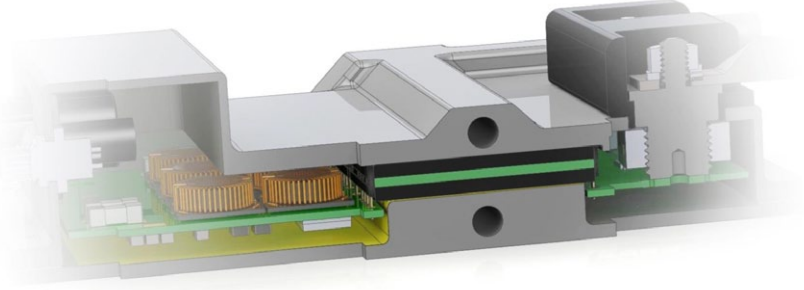
When the game experience of the day was Pong, it was entirely reasonable to try to fascinate young engineers with Basic as the first step on the path to designing such products. When the same age is playing Simcity or Monster Hunter, can we not give them a programming medium that has advanced by a similar amount?

pulse

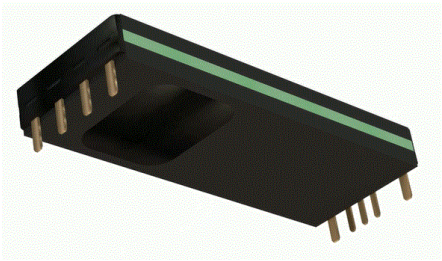
Automated manufacturing yields an even-smaller power module format

Vicor has developed a new construction for its power components and modules that results in a further reduction in package size, and increase in power density, for the engineer using them. Vicor calls the concept ChiP, for "converter housed in package"; it represents an extension of panelised PCB manufacturing techniques to a scale that reflects some of the techniques used by the semiconductor sector for IC manufacturing and wafer handling. Multiple ChiP modules are constructed in parallel, on a high-density PCB substrate, and the entire panel is over-moulded before the individual modules are sawn – in semiconductor-wafer-fashion – into individual units. The over-mould is formed flush with the top of the main magnetic components on the PCB, so that the top of the transformer is exposed as a heat conduction path. This yields a small rectangular package that Vicor is denoting using the same convention as surface-mount passive components; a 1323 package measures 13 x 23 mm, a 2223 measures 22 x 23 mm, and so on: other packages designed so far are 3623, 4623 and 6123. To this, Vicor applies interconnect; the sawing exposes linear copper contact points on two edges of the package, and Vicor attaches conventional pin-outs to them. First units have through-hole terminations: surface-mount variants will be available. This adds 1 – 2 mm to the length of the package, over the bare dimension designation. Potentially, you might obtain the bare module without terminations and use it in a board cut-out, making your own bonds to the edge-connections. Steve Oliver, vice-president of Vicor's VI Chip division, says that this has not been developed, but, "we have it as a concept".

All of Vicor's module architectures and topologies will, over time, be made available in the ChiP package; AC-DC with power-factor correction; isolated bus conversion; DC-DC conversion; buck, boost, and buck-boost regulation; and point-of-load current multiplication (the "DC-DC transformer"). The smallest modules are 4.7 mm in height, set by the magnetics (larger ones are thicker); the package technology can deliver up to 180A, or 1.5 kW, and operation is at up to 430V. Power density is quoted at up to 3 kW/in^3, or up to 850 W/in^2 by area. One of Vicor's illustrations shows a 1323-size VTM current multiplier module that can supply a processor direct from a 48V bus, and that is now small enough to mount very close to the processor socket, without the need for any point-of-load bulk capacitors. You can place this, Vicor says, so that it sits in the exhaust air-flow from the fanned cpu-cooler and gets all of the cooling it needs by that route. The 1323 package housing a sine-amplitude-converter meets the specifications for Intel's forthcoming Haswell processor generation.



With thermal contacts top and bottom, in this concept drawing the ChiP module is liquid-cooled



A ChiP module is built in multiples and sawn apart after moulding

You can use the devices ambient cooled, leaving the wiring-to-PCB as a main heat conduction path; or you can place conduction cooling on both top and bottom surfaces of the package. The illustration below shows a concept drawing for a military-product design using liquid cooling with "sandwich" pressure connections to top and bottom of a ChiP module. Vicor will release products in the ChiP format from mid-2013.

Vicor has also announced an ordering process by which you can configure specific variants of the company's 48-V VI Chip PRM Modules for PoL buck-boost or Factorised Power applications. The PowerBench online tool suite enables you to carry out web-based configuration and simulation for non-standard requirements. The PRM modules act as PoL buck-boost regulators or drive VTM current multipliers. Vicor has previously offered a quick-turnround low-volume ordering process with its "brick" style products, but in that case all the changes made were in hardware, using a highly automated manufacturing process as the basis for the customisation. In this technology, much of the customisation is at a firmware level, using a few standard

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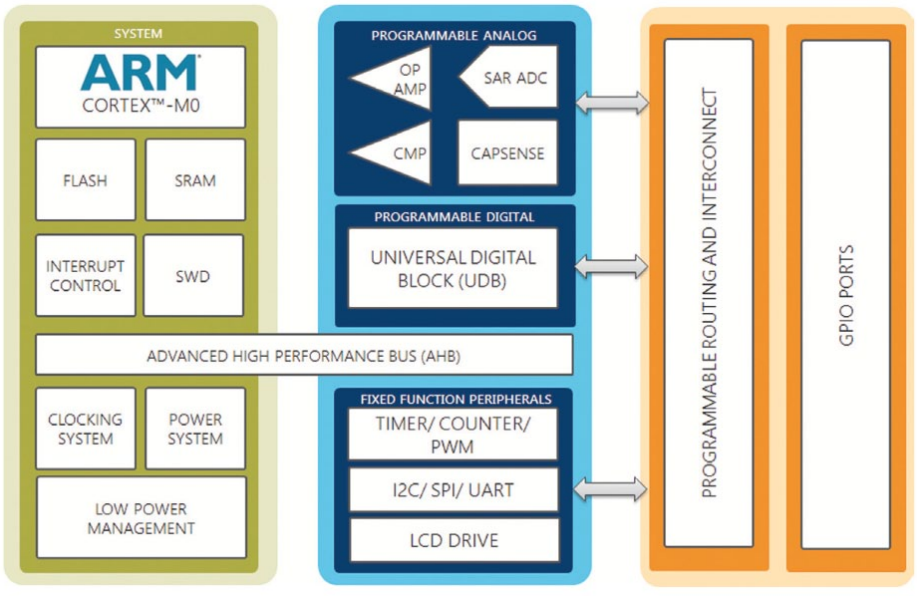
variants from the 48V product line. The PowerBench online tool suite gives you the ability to specify the voltage, current and protection parameters of a PRM module and immediately simulate a module in application-specific operating conditions.
Incorporating Vicor's high-frequency ZVS (zero-voltage-switching) buck-boost technology, customer-configurable VI Chip PRM modules can deliver up to 500W at over 97% efficiency, at power densities of up to 1,700 W/in^3 (103 W/cm^3). Models are available in both full-chip and half-chip packages with input voltage ranges of both 36 - 75 V and 38 - 55 V, and, when used as a PoL buck-boost regulator, provides a user-defined output between 26 V and 52 V. When used with VI Chip VTM current multiplier modules, PRMs efficiently support output voltages from 0.5 V to 55 Vdc.
The online PowerBench tools draw on a complete database of how the (initially, four) customisable devices behave in all conditions. You can simulate startup, shutdown, steady state, load step and input step conditions. The tool will generate a data sheet for "your" module; there is no NRE (non-recurring engineering) cost and modules are shipped in five days. This, says, Vicor's Steve Oliver, can help to get a project back on track where a late change has altered power requirements. A customised part will attract a premium of around 25% over a standard one, Oliver says, adding that in most cases, the designer could not match the cost if constructing the same function from discrete parts.
Vicor, www.vicorpower.com

Cortex-M0 at the core of Cypress' PSoC 4 programmable architecture

With its PSoC 4 architecture Devices, Cypress claims to have the most flexible, lowest-power ARM Cortex-M0-based devices for embedded designs, that is scalable, reconfigurable and that will vie for designs presently fulfilled with 8-, 16-, and 32-bit standalone MCUs.
The PSoC 4 programmable system-on-chip architecture combines Cypress's PSoC analogue and digital fabric and CapSense capacitive touch technology with ARM's Cortex-M0 core, offering analogue performance and a high level of integration, along with access to free PSoC Components. These appear as "virtual chips" represented by icons in the PSoC Creator integrated design environment. The new PSoC 4 device class will challenge proprietary 8-bit and 16-bit microcontrollers (MCUs), along with other 32-bit devices.
In previous enhancements to the pSoC line (pSoC 3, 5), according a Cypress spokesman, the company concentrated on increasing level of integration; this announcement, he said, focusses on reaching a market "sweet spot" enabling the parts to reach a high proportion of designs that are built with 16 or 32-bit microcontrollers. The internal platform of the Cortex M0 core will allow new variants to be produced; its analogue features are also intended to reach the most popular types of design while Cypress says that it may offer higher precision analogue functions in a future release if market demand requires it.
Included is the CapSense capacitive-touch sensing technology for which Cypress claims high level of noise immunity. In addition to capacitive sensing, Cypress envisages applications in field-oriented control (FOC) motor control, temperature sensing, security access, portable medical, and many other applications.
The PSoC 4 architecture offers power leakage of 150 nA while retaining SRAM memory, programmable logic, and the ability to wake up from an interrupt. In stop mode, it consumes only 20 nA while maintaining wake-up capability. It has the widest operating voltage range of any Cortex-M0-based device, enabling full analogue and digital operation from 1.71V to 5.5V. The architecture facilitates integrated, high-performance custom signal chains and provides both configurable analogue and flexible routing.

You design using the PSoC Creator integrated design environment with a graphical interface in which you drag and drop pre-characterised, production-ready analogue and digital IP blocks—PSoC Components—into a single PSoC device. Cypress's platform solution—PSoC 4, PSoC Creator and PSoC Components—simplifies and accelerates the design process and reduces bills of material, Cypress asserts, adding that PSoC solutions bring the flash-based equivalent of a field-programmable ASIC to embedded designs without lead-time or NRE penalties. A single PSoC device can integrate as many as 100 peripheral functions, accelerating cycle time while reducing board space, power consumption, and system cost.
For more information, visit www.cypress.com/go/psoc4



The pSoC4 architecture gives the programmable analogue and digital blocks direct access to the ARM core via the AHB bus

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The AWG 70000 advances each dimension of speed, fidelity and signal duration, Tektronix asserts.

Tektronix uprates high performance AWG to 50 Gsamples/sec

Tektronix' AWG70000 arbitrary waveform generators offer up to 50 Gsamples/sec sample rate performance combined with long waveform memory and deep dynamic range. Tek aims the product at signal generation requirements in defence electronics, high-speed serial, optical networking and advanced research applications.

In addition to its sample – D-to-A conversion – rate the AWG70000 Series has 16 Gsamples of waveform memory, and 10 bits vertical resolution. This means it produces fast, clean signals that can be routed through a receiver or other device under test for long periods of time for truly comprehensive testing. Key parameters for an AWG, Tek says, are speed, dynamic range (leading to a cleaner signal – quantisation noise appears in the noise level of the signal, and wider dynamic range suppresses that better and signal duration without repetition. The AWG 70000 has dynamic range of -75dBc (SFDR). With it you can generate wideband RF signals at up to 20 GHz, serial data signals up to 12 Gbit/sec, and wideband baseband signals to drive optical devices in coherent-optical communications.

At the heart of the design are twin digital/analogue converters developed by Tektronix Component Solutions, and built on IBM's 8HP silicon-germanium process. The 10-bit devices run at 25 Gsamples/sec and are interleaved to achieve the peak conversion rate. Or, you can use them as two channels at their native speed.

Tektronix has recently revealed willingness to make some of its technologies available on the open market; a fast signal processing board released by Curtiss-Wright Controls uses Tek's TADF-430 analogue-to-digital converter alongside Xilinx Virtex FPGAs for high speed signal acquisition and processing. Asked whether the DAC technology in the AWG would similarly become available, a Tek spokesman indicated that this was likely to happen.

As well as interleaving the internal DACs, you can also synchronise multiple AWGs, for example to have a pair provide I and Q signals at 50 Gsamples/sec each, to an I/Q modulator. Tek cites an example at Alcatel-Lucent Bell Labs, where researchers demonstrated 1.5 Terabits per second superchannel transmission over ultra-long-haul optical fibre distances. "The sampling rate of 50 G samples/sec combined with the ability to synchronise two AWGs enabled us to generate 30 GBaud signals per optical carrier, with a data rate of 233 G samples/sec, more than twice the previous record," said S. Chandrasekhar, one of the lead Bell Labs researchers on this project.

You can create signals for the AWG with the RFXpress and SerialXpress software. The former simplifies the creation of IQ, IF and RF signals; adds analogue, digital or custom modulation; and offers specific signal types (for example, chirps) to support radar and OFDM development. The data package creates data patterns with impairments to test receiver jitter, ISI, de- or pre-emphasis, SSC modulation and noise performance. It has a library of patterns for testing of SATA, PCIexpress, SAS, DisplayPort, Fibre Channel, HDMI, USB and MIPI signals: you can also exercise DDR3 signal paths. The AWG70000 offers a two-box solution for HDMI 2.0, supporting four lanes at 6 Gbps per lane. It gives designers the ability to add impairments to waveforms directly, eliminating the dependency on hardware elements to generate the necessary signals.

The display on the front panel shows a simulation of the signal the AWG is commanded to output; the product is also compatible with Tek's high-speed scopes and you can use it to modify and replay captured waveforms.

The AWG70000A Series has single or dual channel variants and pricing starts at €110,100/£91,700.

Tek has also disclosed the target for its next high-speed scope development – next-generation products due in 2014 will deliver real-time bandwidth of 70 GHz, for users in fields such as 400 Gbps and 1 Tbps optical communications and fourth generation serial data communications. The gain in bandwidth performance, with improved signal fidelity, is due in part to the development by Tektronix engineers of a signal processing architecture called Asynchronous Time Interleaving that, "will improve signal-to-noise ratio beyond the frequency interleaving approach used by competing oscilloscope vendors, " according to Tek's CTO Kevin Ilcisin. In traditional frequency interleaving, each analogue-to-digital converter (ADC) in the signal acquisition system only sees part of the input spectrum. With the new technology, all ADCs see the full spectrum with full signal path symmetry. This offers the performance gains available from interleaved architectures while preserving signal fidelity, Tek says.

Tektronix, www.tektronix.com

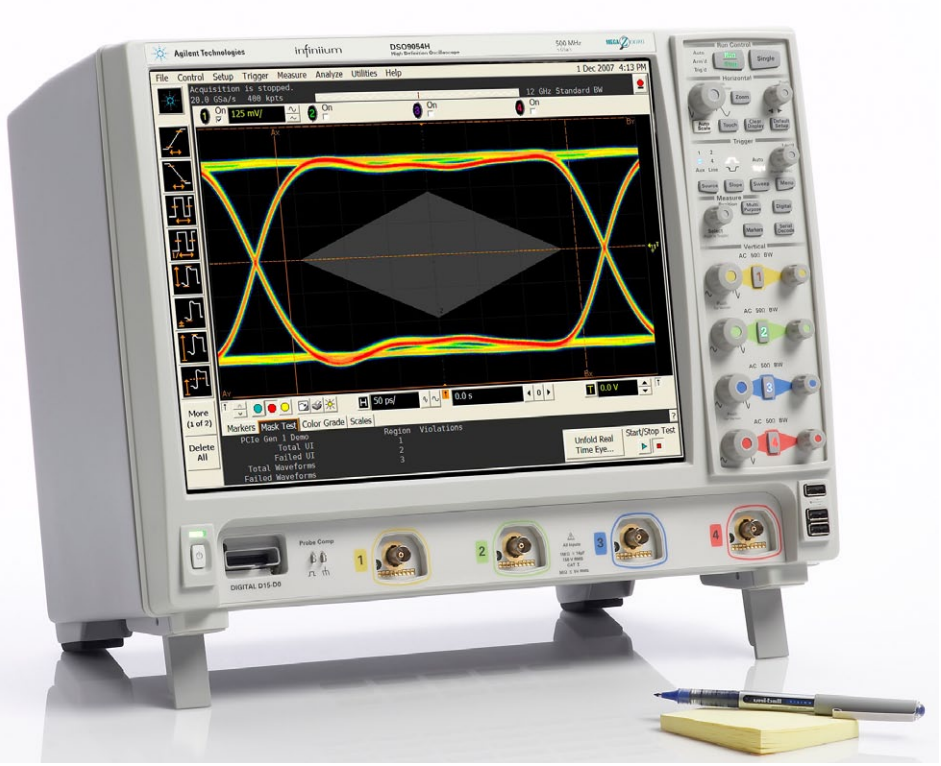
Agilent extends presence in 12-bit scopes with High-Definition models

Agilent Technologies recently announced the Infiniium 9000 H-Series high-definition oscilloscopes, with bandwidths of 250 MHz, 500 MHz, 1 GHz and 2 GHz. They offer up to 12-bit vertical resolution, which represents 16 times the quantisation levels of traditional oscilloscopes with 8 bits of resolution. These scopes also include the industry's deepest standard memory (up to 100 Mpts per channel). In contrast to instruments that base greater signal range on a wider analogue-to-digital converter, Agilent derives the greater effective-number-of-bits (ENOB) from signal processing. "Hypersampling" samples each incoming signal "group" up to 16 times, and linear averaging yields the more accurate representation. Agilent says that his provides significantly better noise performance (signal channel noise floor, relative to displayed full scale) than competing 12-bit scopes. You can use the instrument to resolve small signals that are invisible to an 8-bit scope.

As probing systems also induce measurement noise, Agilent has developed a series of low-noise probes specifically designed to allow engineers to view and analyse small-current signals. The N2820A and N2821A AC/DC current probes offer sensitivity down to 50 µA, with a maximum current range of 5 A. The higher sensitivity is useful for measuring current consumption of battery-powered mobile devices or integrated circuits. The N2820A current probe interface uses a make-before-break connector, offering easy and reliable connecting and disconnecting without interrupting the circuit under test across multiple locations on the target board.

The Agilent 9000 H-Series provides standard memory of up to 100 million points per channel, making it the deepest standard memory in the industry. This memory depth can be upgraded to 500 million points per channel to acquire longer windows of time while retaining fast sample rates. US pricing for the 9000H series starts at $14,950 for the 250-MHz model to $25,000 for the 2-GHz; the probes cost $3000 or $4000 for single- or dual-channel types.

Agilent, www.agilent.com



Signal processing to 12-bit resolution improves resolution of small signal levels.

RMS power detector for RF communications designs spans 10 GHz

Analog Devices' latest RMS power detector features operation up to 10 GHz and a 67 dB measurement range: the ADL5906 TruPwr RMS detector is frequency-versatile and eliminates the need for external input tuning devices, such as a balun (balanced-to-unbalanced signal line transformer). ADI designed the ADL5906 for applications that require an accurate RMS measurement of signal power including communications infrastructure, power amplifier linearisation, point-to-point and point-to-multipoint, cable, military, satellite, instrumentation equipment and ISM band transmitters.

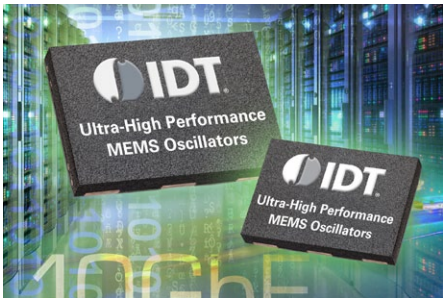
Requiring only a single supply of 5V and a few capacitors, the detector is easy-to-use and capable of being driven with a single-ended or differential input drive. It provides low temperature drift across a -55°C to +125°C range that is highly repeatable from part-to-part, thereby reducing design risk and manufacturing costs.

The device is specified to deliver accurate RMS-to-dc conversion from 10 MHz to 10 GHz; has a single-ended ± 1dB detection range of 67 dB at 2140 MHz, with no balun or external input matching required; and it is tolerant of high peak/average ratio and varying crest factors with response-independent acceptance of waveform types such as GSM/CDMA/W-CDMA/TD-SCDMA/WiMAX/LTE. It will accept inputs from -65 dBm to +8 dBm. The device yields a linear-in-decibels output (that is it has in-built linear to logarithmic conversion), scaled 55 mV/dB (1.1V per decade) at 2140 MHz; has temperature stability of < ±1 dB from -40°C to +85°C; powers-down to 250 µA; and is pin-compatible with the ADL5902 and AD8363 TruPwr detectors. It comes in a 4mm x 4mm 16-lead LFCSP package and costs $5.59 (1000).

More; www.analog.com/adl5906

pulse

Low-jitter MEMS oscillators with integrated frequency margining



MEMS piezo-electric oscillators offer a drop-in upgrade for quartz in critical applications.

Integrated Device Technology's 4H LVDS/LVPECL MEMS oscillators with 100 fsec typical phase jitter and adaptable output frequency reduce BER in high-performance 10GbE and networking applications. IDT claims the industry's first differential MEMS oscillators with 100 femtosecond (fsec) typical phase jitter performance and integrated frequency margining capability. The extremely low phase jitter and adaptable output frequency of IDT's high-performance oscillators reduce bit error rate (BER) in 10 gigabit Ethernet (10GbE) switches, routers, and other related networking equipment.

The IDT 4H performance MEMS oscillators feature a differential LVDS/LVPECL output and the lowest phase jitter in their product class (100 fsec at 1.875 - 20 MHz and sub-300 fsec at 12kHz - 20 MHz), satisfying the low-jitter chipset requirements of high-performance networking applications. Integrated frequency margining capability enables customers to fine-tune the oscillator frequency during operation in the application by up to ±1000 ppm, minimising BER and facilitating margin testing. The MEMS oscillators are available in multiple package sizes including the smaller 3225 (3.2 x 2.5 mm) to save board space and cost in densely populated applications. IDT believes it is only supplier to offer this combination of MEMS oscillator performance, features, and small package size.

Frequency margining capability enables a technique known as 'plus-PPM clocking'. This technique clocks systems at a slightly higher frequency, allowing OEMs to reduce BER and resulting packet losses in networking applications. IDT's device allows hundreds of offset frequencies that can be generated after the selection of any base frequency up to 625 MHz – even on final production systems.

The 4H MEMS oscillators use IDT's piezoelectric MEMS (pMEMS) resonator technology to provide a high-frequency source. IDT MEMS oscillators claim 40 times better reliability than quartz with no activity dips, no zero-time failures, higher jitter resistance to EMI, and excellent shock and vibration resistance, making them an upgrade solution for traditional quartz-based oscillators. The IDT 4H MEMS oscillators are currently sampling in standard 7.0 x 5.0 mm, 5.0 x 3.2 mm and 3.2 x 2.5 mm VFQFPN packages. Most standard frequencies are available, and custom frequencies can be configured by request.

IDT, www.idt.com/go/MEMS

Shape-based router executes automatic custom mixed-signal IC net routing

Synopsys has announced the Galaxy Custom Router, to work with its IC Compiler Custom solution, and that adds new analogue and mixed-signal routing technology, with automated routing for custom nets, such as shielded buses, and differential pairs: the tool supports 20-nm, and smaller, process technology rules, including double-patterning. Added to the Galaxy Platform, the Galaxy Custom Router provides automatic routing for complex high-speed digital and mixed-signals nets that require carefully crafted, high-quality layouts, such as shielded buses or nets, differential pairs, twisted pairs and matched resistance and capacitance (RC) routing. This new shape-based router delivers, Synopsys claims, two to five times productivity improvements over manual efforts and is ready for use with advanced designs by offering support for 20-nanometer (nm) and smaller process technology design rules, including double-patterning.

The router enables IC Compiler users to create high-quality routing patterns for difficult routing tasks, such as differential pair routing, shielded routing (including bus and differential pair shielding), matched RC routing, river routing and point-to-point coaxial routing. River routing is where each net route is completed in a single layer; you can use multiple layers in river routing to stack routes through congested channels, each individual net stays on one layer. Other features include complex signal shielding of river-routed paths in parallel, tandem and coaxial layouts; differential-pair, star and balanced routing; matched routing, clock tree routing; shielding in parallel, tandem, and coaxial modes of buses, differential pairs and scalar nets; and resistance, capacitance (RC) and length matching. You can place shielding wires around signal wires in interleaved or double-interleaved styles, that is with one or two shield wires between the bit nets.

The router supports features for analogue block-level routing, including matched route, differential pair, triplet, star and balanced routing. These routes may also be shielded or twisted using several different styles. Routes may be matched either by length or by resistive and capacitive values. For differential pair or triplet routing, two or three pins are routed together, according to the spacing constraint, with matched length: pairs can be shielded and/or twisted, with the option of a 90-degree or 45-degree twist. Parallel shielding places shield wires either side of a signal line: tandem shielding places them above and below in adjacent layers; and coaxial shielding "wraps" a signal line by doing both.

Users can pre-route sensitive nets using a rich set of custom routing options and continue with IC Compiler to complete the physical implementation. Galaxy Custom Router supports advanced process technology nodes, including 20-nm. It adheres to constraints specified in IC Compiler, including default and non-default design rules, routing grids, route keep-outs, route blockages and route guides.

"Increasingly, mixed-signal and digital designs require hand-crafted-quality routing for sensitive analog and high-speed digital signals," said Paul Lo, senior vice president and general manager of the Synopsys Analog/Mixed-Signal Group. "Galaxy Custom Router is a key technology for addressing this need, and a significant milestone toward realizing our vision of a unified solution for digital and custom system-on-chip design."

More at www.synopsys.com

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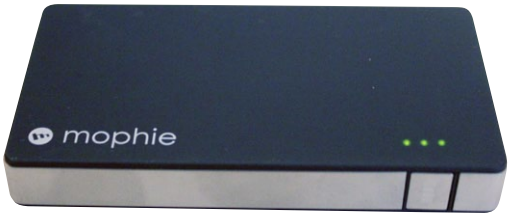
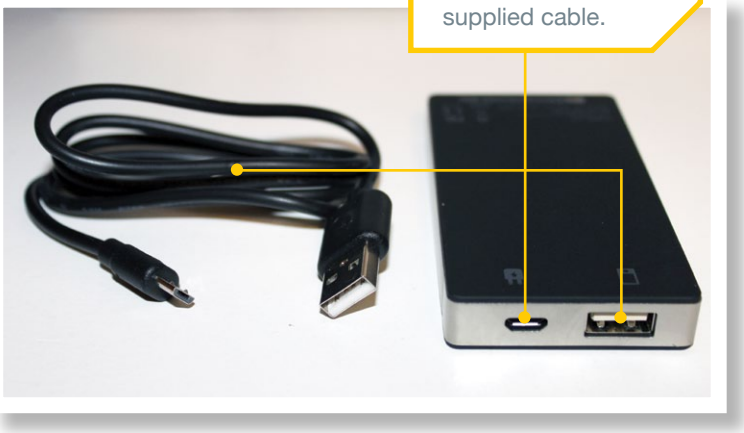
Cell-phone charger: nice idea done right



Back in November 2012, EDN Brand Director Patrick Mannion published a teardown of a cell-phone battery charger (www.edn.com/4401998). The design was not well done and received bad reviews. Redemption! I recently acquired a Mophie juice pack powerstation mini smartphone and USB-device battery charger that not only negates the previous teardown fiasco but also demonstrates the ability to provide more than twice the battery life to your smartphone while still keeping a low-profile shape that slips right into your pocket.

Mophie, a California-based designer and manufacturer of mobile intelligent devices and accessories, developed the juice pack, the first ever "Works with iPhone" portable battery case certified by Apple. I contacted the company via e-mail for its help clarifying this design as well as the component types. It has not yet responded, so I give you my educated guesses. EDN readers are encouraged to weigh in with their own thoughts and expertise.

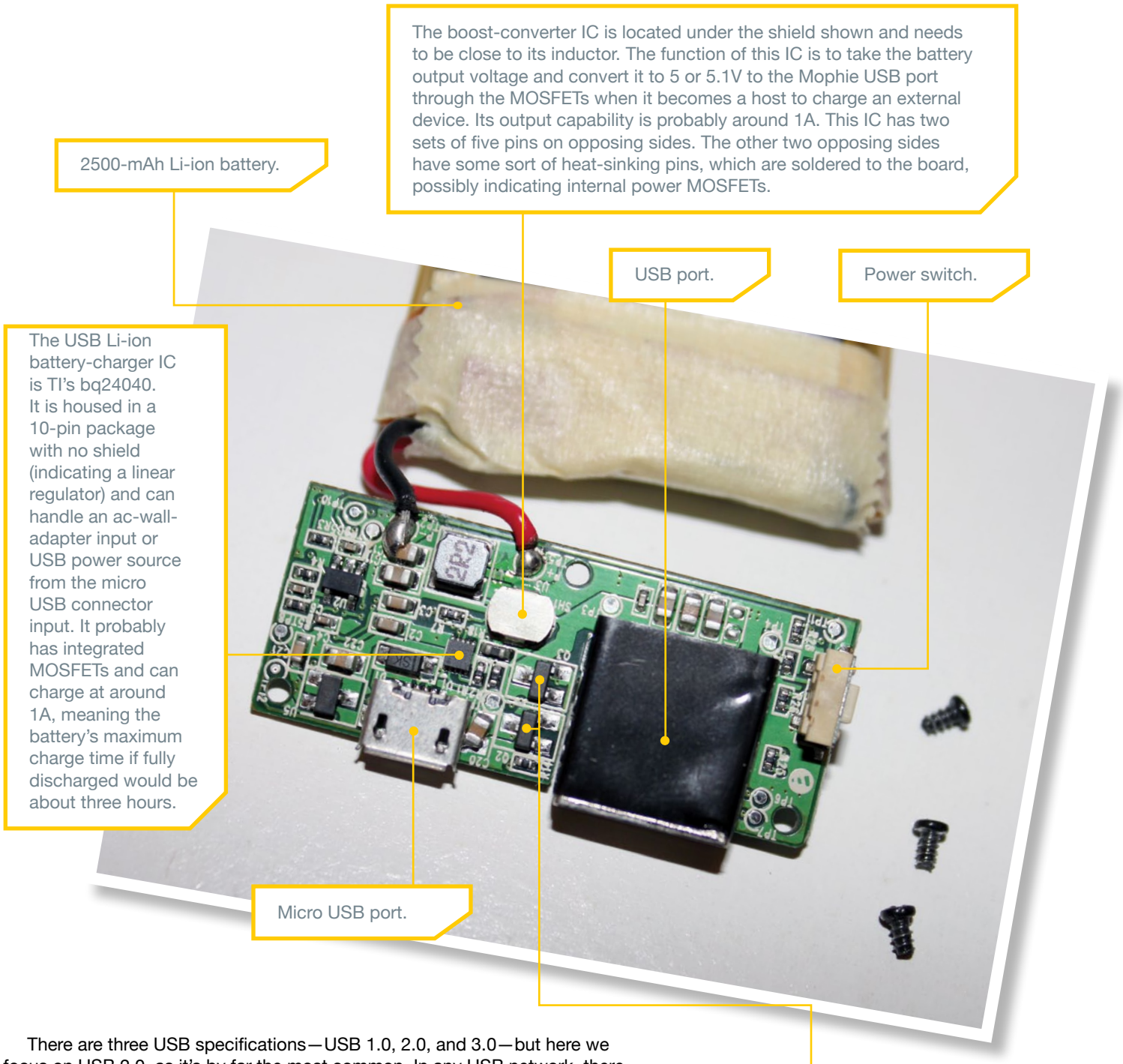
The micro USB and standard USB ports on the side of the case were quite secure. I tested them many, many times, inserting and extracting the connectors from the supplied cable.



I think a Microchip MCU is located under the shield shown. The microcontroller usually controls the housekeeping; provides charge control for the USB battery-charger IC, IC_1; controls the four LEDs for the charge-status indicator; has I^2C bus capability if needed for IC_1; and controls the power MOSFETs. The Microchip part is unusual for a few reasons. It appears to have a Microchip symbol and only a date code, with no sign of a part number. There are eight pins on two sides opposing one another. On the other two sides are what look like eight pins—six of the eight are cut off and two are connected to the PCB, on each opposing side. Sometimes manufacturers provide early samples of a new die not yet fully qualified in a nonstandard package, but I am not sure.

2500-mAh lithium-ion battery.

Power-indicator LEDs with rubber elastomer.



There are three USB specifications—USB 1.0, 2.0, and 3.0—but here we focus on USB 2.0, as it's by far the most common. In any USB network, there is one host and one device. In this case, the Mophie juice pack is the host, and your smartphone/tablet/camera is the device. Power always flows from the host to the device, but data can flow in both directions. In this case, the USB port is a dedicated charging port.

A USB socket has four pins, and a USB cable has four wires. The inside pins carry data (D+ and D–); the outside pins provide a 5V power supply. In terms of actual current (milliamps, or mA), there are three kinds of USB ports dictated by the current specs: a standard downstream port, a charging downstream port, and a dedicated charging port. The first two can be found on your computer (and should be labeled as such); the third kind applies to "dumb" wall chargers. In the USB 1.0 and 2.0 specs, a standard downstream port is capable of delivering up to 500 mA (0.5A); in USB 3.0, it moves up to 900 mA (0.9A). The charging downstream and dedicated charging ports provide up to 1500 mA (1.5A).

BY HENRY J ZHANG • LINEAR TECHNOLOGY CORP

PCB-layout considerations for nonisolated switching power supplies

A GOOD LAYOUT DESIGN OPTIMIZES EFFICIENCY, ALLEVIATES THERMAL STRESS, AND MINIMIZES THE NOISE AND INTERACTIONS AMONG TRACES AND COMPONENTS. IT ALL STARTS WITH THE DESIGNER'S UNDERSTANDING OF THE CURRENT-CONDUCTION PATHS AND SIGNAL FLOWS IN THE SUPPLY.

The best news when you power up a prototype supply board for the very first time is that it not only works, but also runs quiet and cool. Unfortunately, that is not always the case.

A common problem with switching power supplies is "unstable" switching waveforms. Sometimes, waveform jitter is so pronounced that the magnetic components generate audible noise. If the problem is related to the printed-circuit-board layout, identifying the cause can be difficult. That is why proper PCB layout at the early stage of a switching-power-supply design is critical.

The power-supply designer best understands the technical details and functional requirements of the supply in the final product. Thus, from the outset of the board-design project, the power-supply designer should work closely with the PCB layout designer on the critical supply layout.

A good layout design optimizes supply efficiency and alleviates thermal stress; most important, it minimizes the noise and interactions among traces and components. To achieve those goals, the designer must understand the current-conduction paths and signal flows in the switching power supply. Keep the following design considerations in mind to achieve a proper layout design for nonisolated switching power supplies.

THE LAYOUT PLAN

To achieve the best voltage regulation, load transient response, and system efficiency for an embedded dc/dc supply on a large board, locate the supply output near the load de-vices to minimize the interconnection impedance and the conduction voltage drop across the PCB traces. Ensure good airflow to limit the thermal stress; if forced-air cooling is available, locate the supply close to the cooling fan.

In addition, the large passive components, such as inductors and electrolytic capacitors, should not block the airflow to low-profile, surface-mount semiconductor components such as power MOSFETs or PWM controllers. To prevent the switching noise from upsetting other analog signals in the system, avoid routing sensitive signal traces underneath the supply if possible; otherwise, you will need an internal ground plane between the power-supply layer and the small-signal layer for shielding.

It's important to plan out your power-supply location and board real-estate requirements during the system's early design and planning phase. Designers sometimes ignore that advice and focus first on more "important" or "exciting" circuits on the big system board. Treating power management as an afterthought and relegating the supply to whatever space is left on the board are contrary to achieving an efficient and reliable power-supply design.

For multilayer boards, it is highly desirable to place the dc ground or dc input- or output-voltage layers between the high-current, power-component layer and the sensitive, small-signal trace layer. The ground or dc voltage layers provide ac grounds to shield the small-signal traces from noisy power traces and power components.

As a general rule, the ground or dc voltage planes of a multilayer PCB should not be segmented. If you find that such segmentation is unavoidable, minimize the number and length of traces in those planes, and route the traces in the same direction as the high-current-flow direction to minimize the impact.

Figures 1a and 1c illustrate undesirable layer arrangements for six- and four-layer switching-power-supply PCBs, respectively. The configurations sandwich the small-signal layer between the high-current power layer and the ground layer, thereby increasing capacitive-noise coupling between the high-current/voltage power layer and the analog small-signal layer.

In figures 1b and 1d, respectively illustrating desirable layer arrangements for minimizing noise coupling in six- and four-layer PCB designs, the ground layers shield the small-signal layers. It is important always to have a ground layer next to the outside power-stage layer, and it is desirable to use thick copper for the external high-current power layers to minimize PCB conduction loss and thermal impedance.

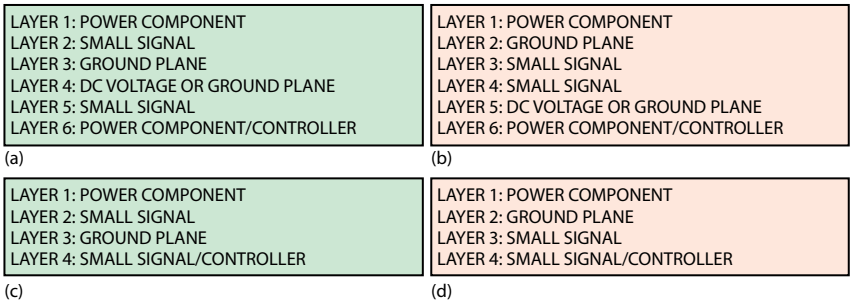


Figure 1 Undesirable layer arrangements for six- (a) and four-layer (c) switching-power-supply PCBs sandwich the small-signal layer between the high-current power layer and the ground layer. In desirable arrangements for six- (b) and four-layer (d) designs, the ground layers shield the small-signal layers.

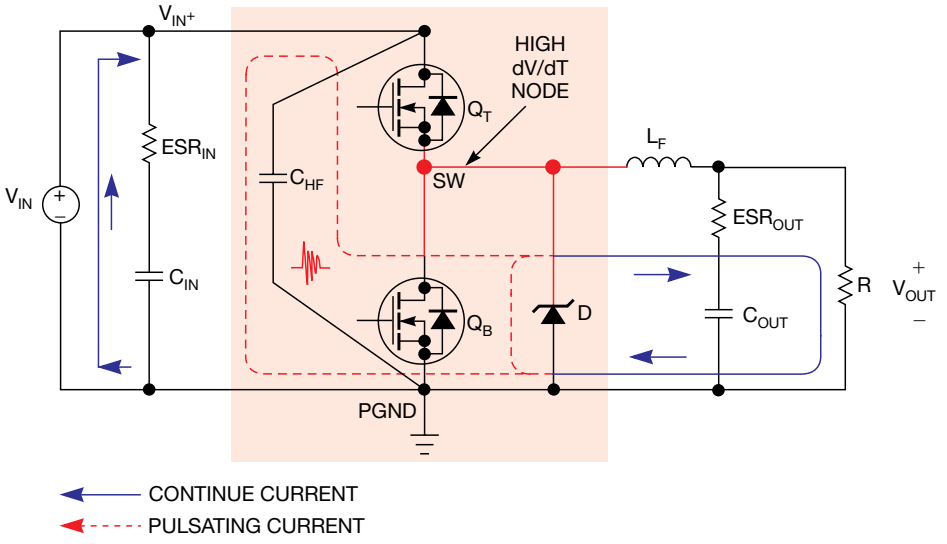


Figure 2 *The solid line represents the continuous-current paths in a synchronous buck converter; the dashed line represents the pulsating (switching)-current paths.*

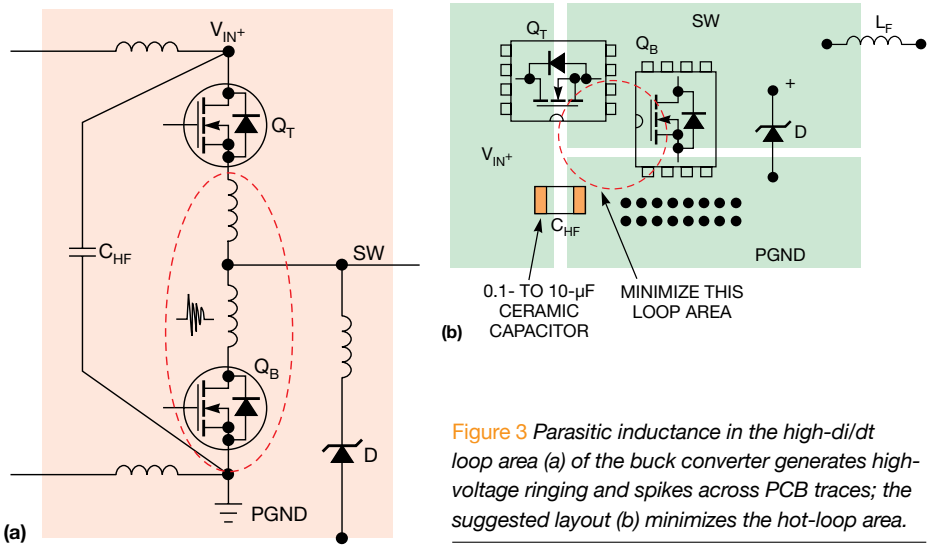


Figure 3 *Parasitic inductance in the high-di/dt loop area (a) of the buck converter generates high-voltage ringing and spikes across PCB traces; the suggested layout (b) minimizes the hot-loop area.*

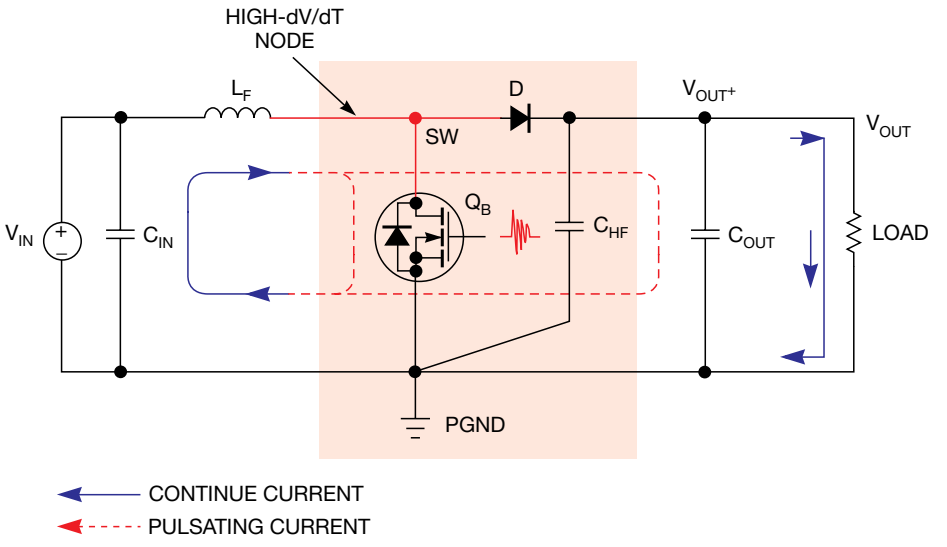


Figure 4 *The continuous- and pulsating-current paths in the boost converter are shown. The high-frequency ceramic capacitor, C_{HF}, should be placed on the output side close to the MOSFET, Q_B, and boost diode, D.*

POWER-STAGE LAYOUT

A switching-power-supply circuit can be divided into the power-stage circuit and the small-signal control circuit. The power-stage circuit includes the components that conduct high current; in general, you would place those components first and then place the small-signal control circuitry in specific spots in the layout.

The large current traces should be short and wide to minimize PCB inductance, resistance, and voltage drop. This setup is especially critical for the traces with high-di/dt pulsating-current flow.

Figure 2 identifies the continuous- and pulsating-current paths in a synchronous buck converter; the solid line represents the continuous-current paths, and the dashed line represents the pulsating (switching)-current paths. The pulsating-current paths include the traces connected to the input decoupling ceramic capacitor, C_{HF}; the top control FET, Q_T; and the bottom synchronous FET, Q_B, with its optional, paralleled Schottky diode.

Figure 3a shows the parasitic PCB inductors in the high-di/dt current paths. Because of the parasitic inductance, the pulsating-current paths not only radiate magnetic fields but also generate high-voltage ringing and spikes across the PCB traces and MOSFETs. To minimize PCB inductance, lay out the pulsating-current loop (hot loop) so that it has a minimum circumference and comprises traces that are short and wide.

The high-frequency decoupling capacitor, C_{HF}, should be a 0.1- to 10-µF, X5R- or X7R-dielectric ceramic capacitor with very low ESL (effective series inductance) and ESR (equivalent series resistance). Higher-capacitance dielectrics (such as Y5V) can allow a large reduction in capacitance over voltage and temperature and thus are not preferred materials for C_{HF} use.

Figure 3b provides a layout example for the critical pulsating-current loop in the buck converter. To limit resistive voltage drops and the number of vias, place power components on the same side of the board, with power traces routed on the same layer. When it is necessary to route a power trace to another layer, choose a trace in the continuous-current paths. When using vias to connect PCB layers in the high-current loop, deploy multiple vias to minimize via impedance.

Figure 4 shows the continuous- and pulsating-current loops in the boost converter. In this case, you should place the high-frequency ceramic capacitor, C_{HF}, on the output side close to the MOSFET, Q_B, and boost diode, D.

Figure 5 provides a layout example for the pulsating-current loop in the boost converter. It is critical to minimize the loop formed by the switch, Q_B, recti-

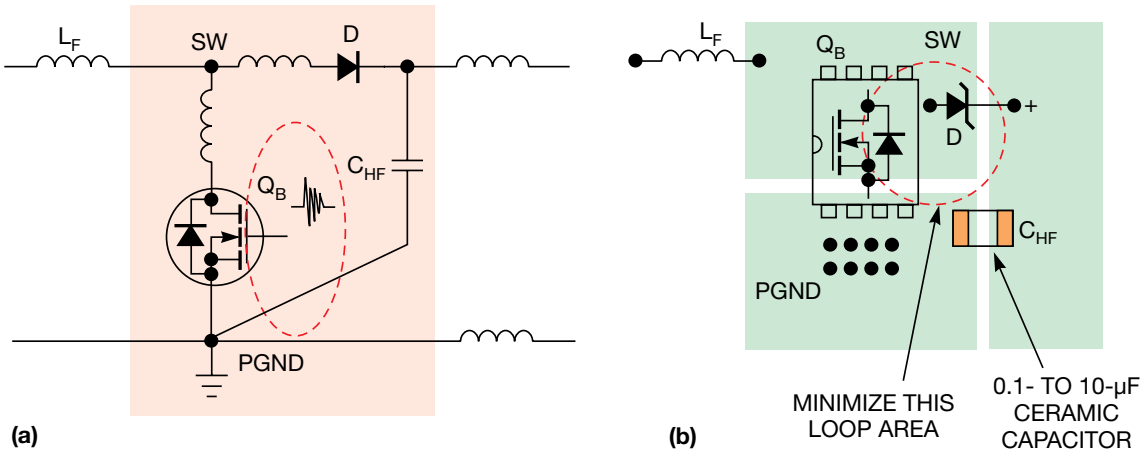
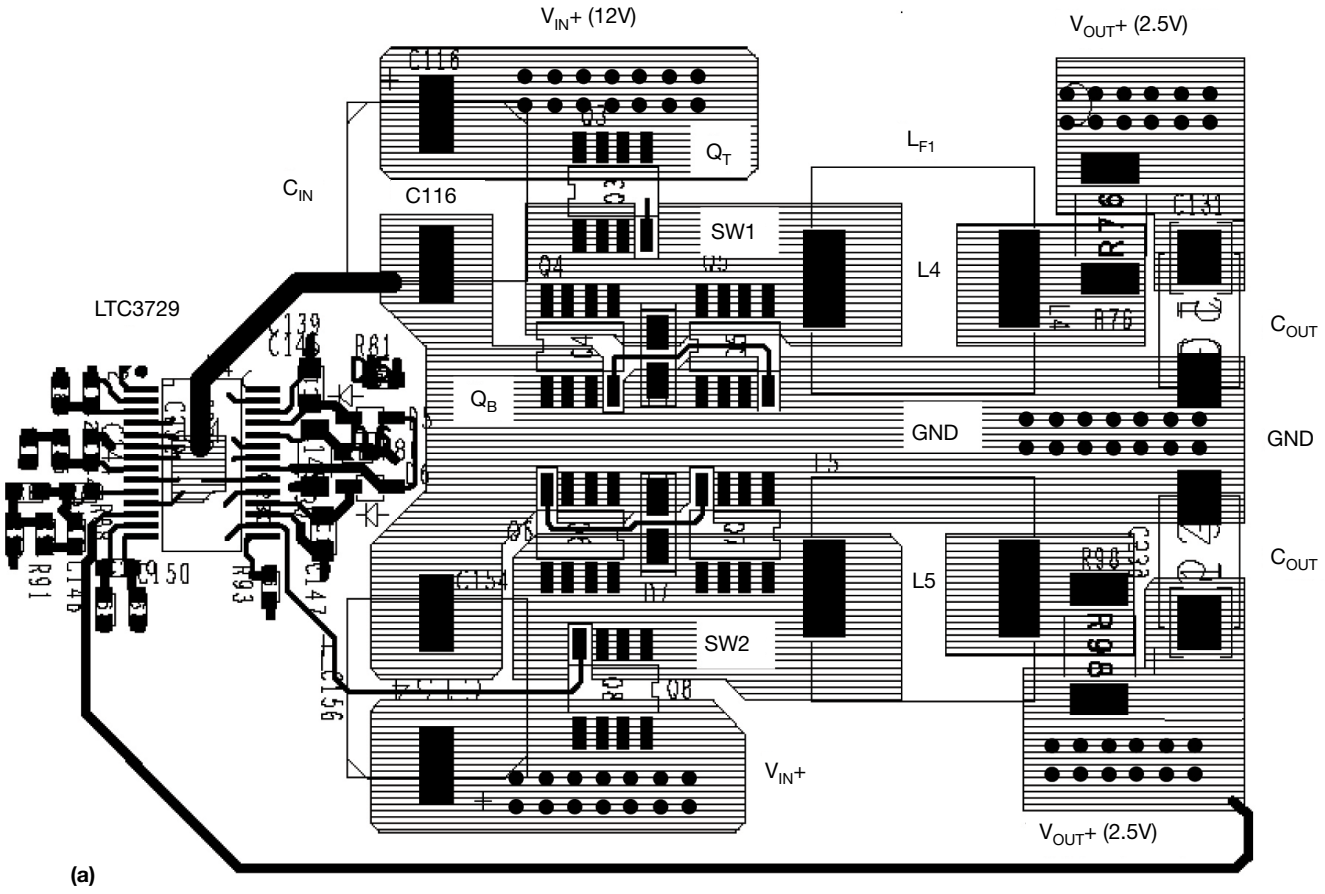


Figure 5 *The hot-loop and parasitic PCB inductors in the boost converter are shown (a); the suggested layout (b) minimizes the hot-loop area.*



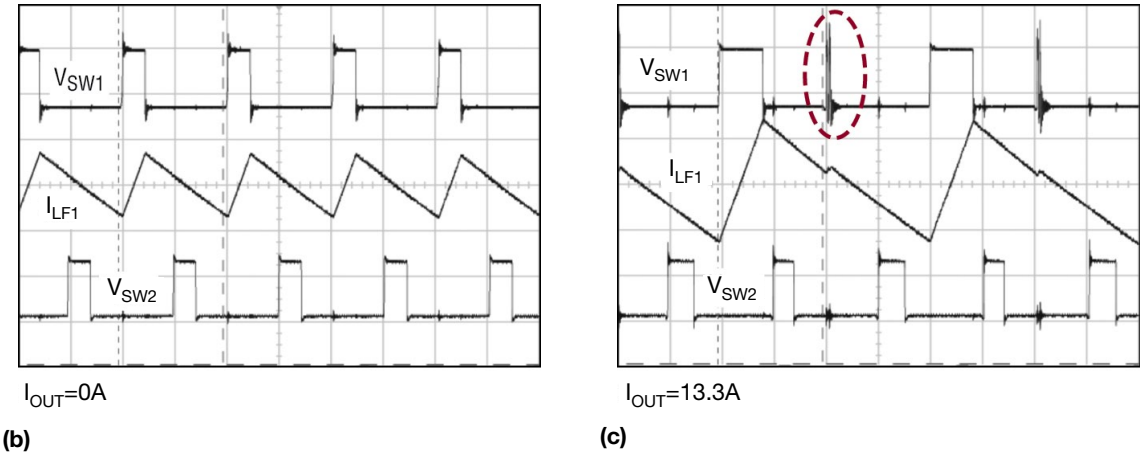
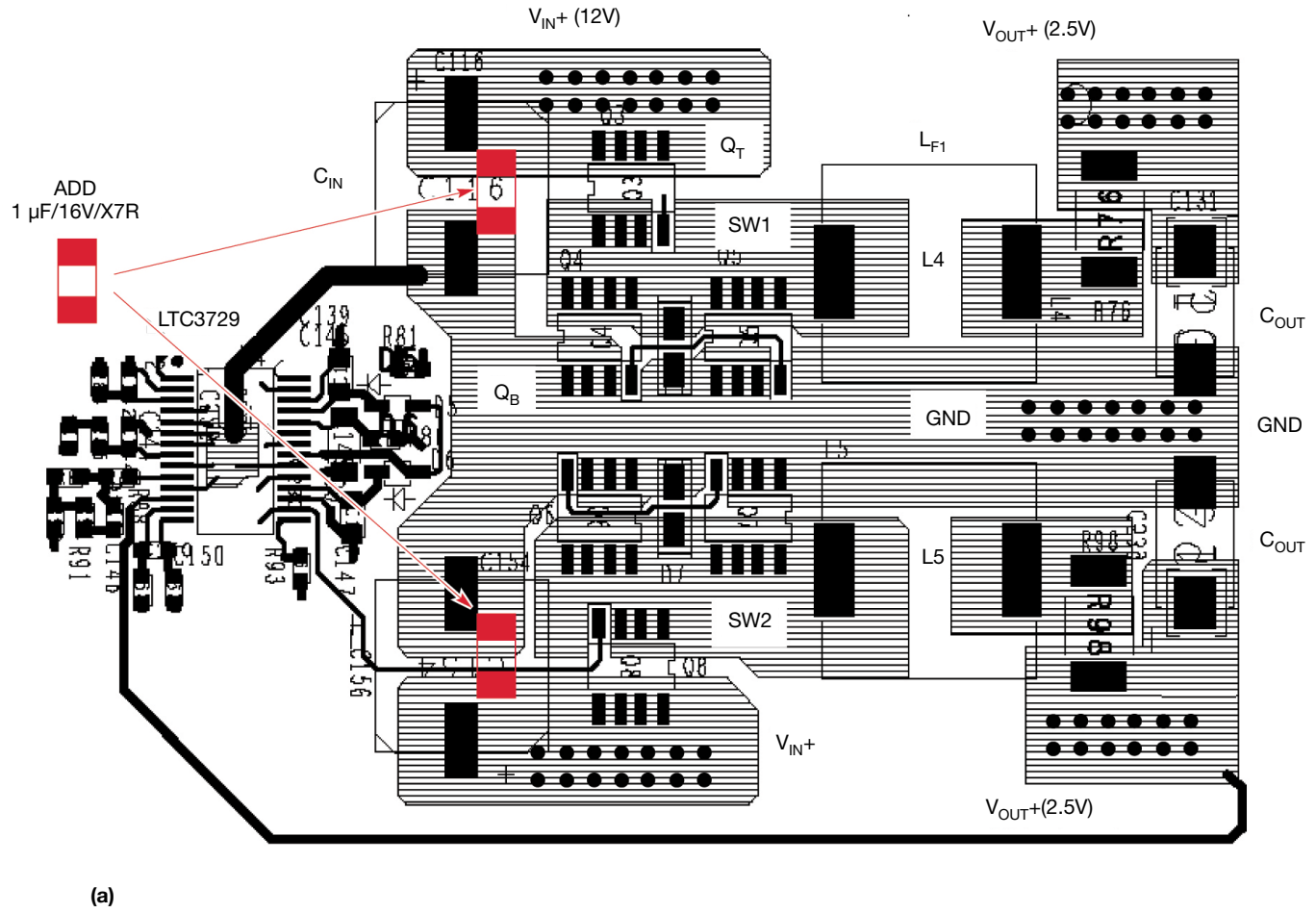
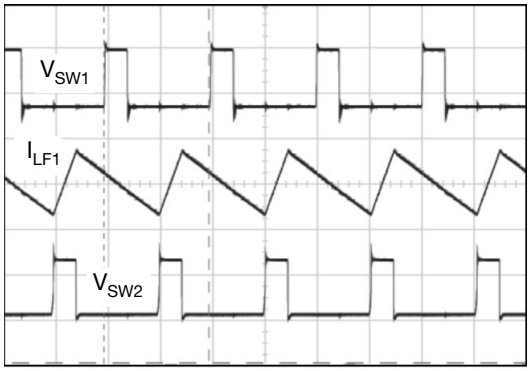


Figure 6 *This two-phase, 2.5V/30A output buck converter (a) has a noise problem: Switching waveforms are stable at no load (b), but the SW1 waveform misses cycles when load current exceeds 13A (c).*

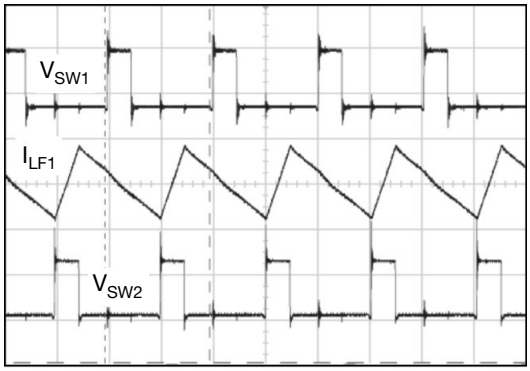


(a)



IOUT=0A

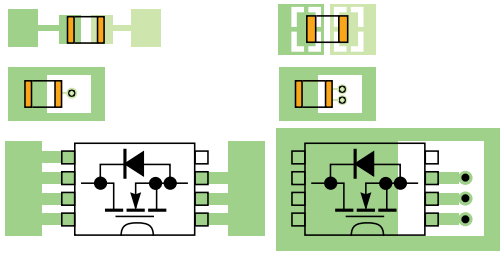
(b)



IOUT=30A

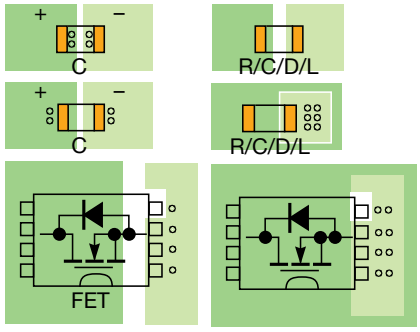
(c)

Figure 7 *Adding two 1-µF, high-frequency input capacitors (a) solves the noise problem, as the switching waveforms at zero load (b) and 30A load (c) show.*



CONNECTED VIA

(a)



CONNECTED VIA

(b)

Figure 8 *Unnecessary use of thermal-relief land patterns (a) increases the interconnection impedance of power components; in the recommended land pattern (b), the positive and negative vias are kept as close to each other as possible to minimize ESL.*

fier diode, D, and high-frequency output capacitor, C_{HF}.

To emphasize the importance of the decoupling capacitor, figures 6 and 7 provide an example of a synchronous buck circuit. Figure 6a shows the layout of a dual-phase, $12V_{IN}$ to $2.5V_{OUT}$/30A max, synchronous buck supply using the LTC3729 two-phase, single-V_{OUT} controller IC. The waveforms for switching nodes SW1 and SW2 and output inductor current I_{LF1} are stable at no load (Figure 6b). If the load current exceeds 13A, however, the SW1 node waveform starts missing cycles. The problem becomes even worse with higher load current (Figure 6c).

Adding two 1-µF high-frequency ceramic capacitors—one on each channel's input side—solves the problem by separating and minimizing the hot-loop area of each channel. The switching waveform is stable even with maximum load current up to 30A.

HIGHER-CAPACITANCE DIELECTRICS CAN ALLOW A LARGE REDUCTION IN CAPACITANCE OVER VOLTAGE AND TEMPERATURE AND THUS ARE NOT PREFERRED MATERIALS FOR C_{HF} USE.

HIGH-DV/DT SWITCHING AREA

In figures 2 and 4, the SW voltage swings with a high dv/dt rate between V_{IN} (or V_{OUT}) and ground. This node is rich in high-frequency noise components and is a strong source of EMI noise. To minimize the coupling capacitance between the switching node and other noise-sensitive traces, you would minimize the SW copper; however, to conduct high inductor current and provide a heat sink to the power MOSFET, the SW-node PCB area cannot be made too small. It is usually preferable to place a ground copper area underneath the switching node to provide additional shielding.

In a design without external heat sinks for surface-mounted power MOSFETs and inductors, the copper area must be sufficient for heat sinking. For a dc voltage node, such as input/output voltage and power ground, it is desirable to make the copper area as large as possible.

Multiple vias are helpful in further reducing thermal stress. For high-dv/dt switching nodes, determining the proper size for the switching-node copper area involves a design trade-off between minimizing dv/dt-related noise and providing good heat-sinking capability for the MOSFETs.

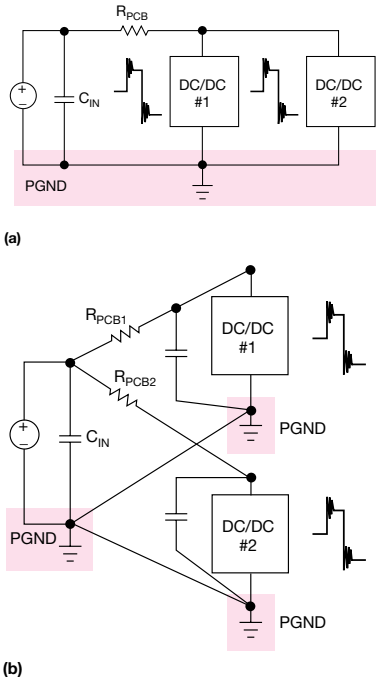


Figure 9 *When multiple onboard switching supplies share the same input-voltage rail (a), separate the input-current paths among the supplies for a more desirable setup (b).*

POWER LAND PATTERNS

It is important to pay attention to the land (or pad) pattern of power components, such as low-ESR capacitors, MOSFETs, diodes, and inductors. Figures 8a and 8b show examples of undesirable and desirable power-component land patterns, respectively.

For a decoupling capacitor, the positive and negative vias

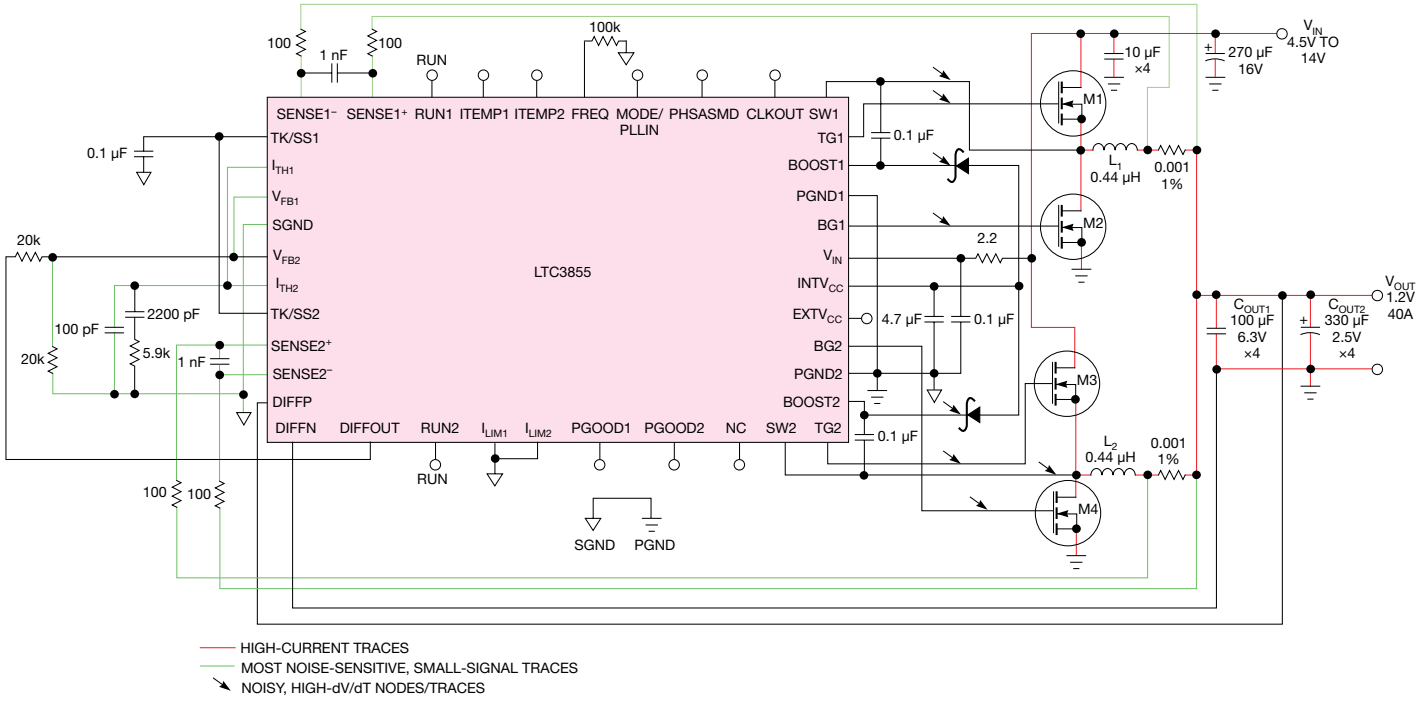


Figure 10 *Using different colors in the schematic to indicate the different types of traces, as was done here for the LTC3855 buck converter, will help the PCB designer distinguish among them.*

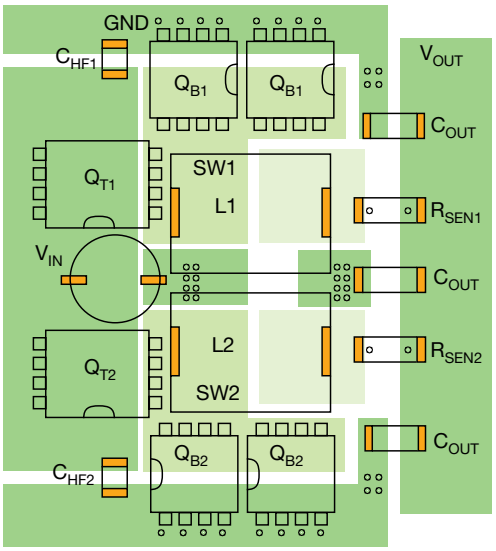


Figure 11 *In this power-stage layout of a dual-phase, single-V_{OUT} buck converter, a solid power-ground-plane layer is placed just underneath the power-component layer.*

should be as close to each other as possible to minimize PCB ESL (Figure 8b). This is especially effective for capacitors with low ESL. Large-valued, low-ESR capacitors are usually more expensive; improper land patterning and poor routing can degrade their performance and thus increase overall cost. In general, the desired land patterns reduce PCB noise, reduce thermal impedance, and minimize trace impedance and voltage drops for the high-current components.

One common mistake in high-current power-component layout is the improper use of thermal-relief land patterns, as Figure 8a shows. Unnecessary use of thermal-relief land patterns increases the interconnection impedance of power components, resulting in higher power losses and decreasing the decoupling effect of low-ESR capacitors. If you use vias to conduct high current in your layout, be sure to use them in sufficient numbers to minimize via impedance. Further, do not use thermal relief for those vias.

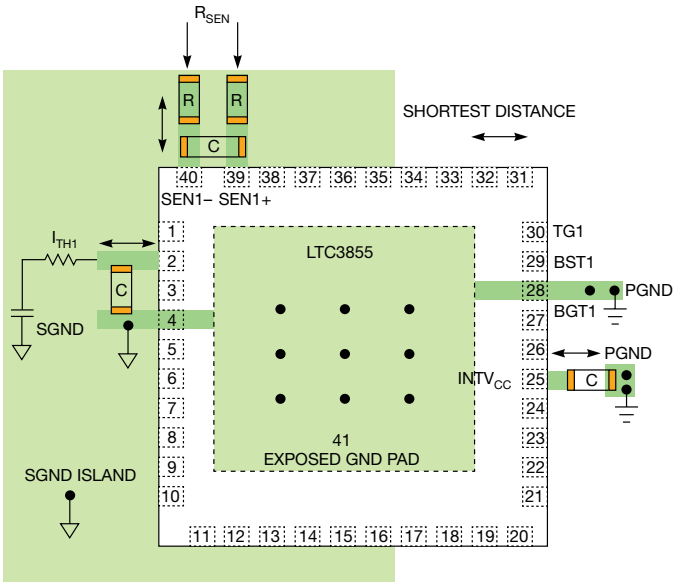


Figure 12 *In the preferred ground-separation scheme for the LTC3855 supply, the IC has an exposed GND pad, which should be soldered down to the PCB to minimize electrical and thermal impedance. Several critical decoupling capacitors should be next to the IC pins.*

Figure 9 shows an application with several onboard switching supplies sharing the same input-voltage rail. When those supplies are not synchronized to each other, it is necessary to separate the input current traces to avoid common-impedance noise coupling between different power supplies. It is less critical to have a local input-decoupling capacitor for each power supply.

For a PolyPhase single-output converter, having a symmetric layout for each phase helps to balance thermal stresses.

LAYOUT DESIGN EXAMPLE

Figure 10 provides a design example of a 4.5V to 14V_{IN} to 1.2V/40A max dual-phase synchronous buck converter using the LTC3855 PolyPhase current-mode step-down controller. Before starting your PCB layout, one good practice is to use different colors in the schematic to highlight the high-current traces; the noisy, high-dv/dt traces; and the sensitive, small-signal traces. Such delineation will help PCB designers distinguish among the traces.

Figure 11 shows a power-stage layout example for the power-component layer of this 1.2V/40A supply. In this figure, Q_T is the top-side control MOSFET and Q_B the bottom-side synchronous FET. An optional Q_B footprint is added for even more output current. A solid power-ground-plane layer is placed just underneath the power-component layer.

CONTROL-CIRCUITRY LAYOUT

Keep the control circuitry away from the noisy, switching copper areas. It is preferable to locate the control circuitry close to the V_{OUT}+ side for the buck converter and close to the V_{IN}+ side for the boost converter, where the power traces carry continuous current.

If space allows, locate the control IC a small distance (0.5 to 1 in.) from the power MOSFETs and inductors, which are noisy and hot. If space constraints force you to locate the controller close to power MOSFETs and inductors, take special care to isolate the control circuitry from the power components with ground planes or traces.

The control circuitry should have a separate signal (analog)-ground island from the power-stage ground. If there are separate SGND (signal ground) and PGND (power ground) pins on the controller IC, you should route them separately. For controller ICs that have integrated MOSFET drivers, the small-signal section of the IC pins should use the SGND (Figure 12).

Only one connection point is required between the signal and power grounds. It is desirable to return the signal ground to a clean point of the power-ground plane. Connecting both ground traces just under the controller IC can accomplish the two grounds. Figure 12 shows the preferred ground separation of the LTC3855 supply. In this example, the IC has an exposed ground pad. It should be soldered down to the PCB to minimize electrical and thermal impedance. Multiple vias should be placed on the ground-pad area.

IF SPACE ALLOWS, LOCATE THE CONTROL IC A SMALL DISTANCE (0.5 TO 1 IN.) FROM THE POWER MOSFETS AND INDUCTORS, WHICH ARE NOISY AND HOT.

The decoupling capacitors for the controller IC should be physically close to their pins. To minimize connection impedance, it is preferable to connect the decoupling capacitors directly to the pins without using vias. As shown in Figure 12, the LTC3855 pins that should have their decoupling capacitors closely located are the current-sensing pins, $Sense^+/Sense^-$; compensation pin, I_{TH}; signal-ground pin, SGND; feedback-voltage divider pin, FB; IC V_{CC} voltage pin, $INTV_{CC}$; and power-ground pin, PGND.

LOOP AREA AND CROSSTALK

Two or more adjacent conductors can be coupled capacitively. High dv/dt on one conductor will couple currents to another through the parasitic capacitor. To reduce the noise coupling from the power stage to the control circuitry, keep the noisy switching traces far from the sensitive small-signal traces. If possible, route the noisy traces and sensitive traces on different layers, using an internal ground layer for noise shielding.

The FET-driver TG, BG, SW, and BOOST pins on the LTC3855 controller have high-dv/dt switching voltages. The LTC3855 pins connected to the most sensitive small-signal nodes are Sense$^+$/Sense$^-$, FB, I_{TH}, and SGND. If the layout routes sensitive signal traces close to high-dv/dt nodes, you must insert ground traces or a ground layer between the signal traces and high-dv/dt traces to shield the noise.

Using short and wide traces to route gate-drive signals helps minimize impedance in gate-drive paths. In Figure 13, you should route top FET-driver traces TG and SW together with a minimum loop area to minimize inductance and high-dv/dt noise. Similarly, route bottom FET-driver trace BG close to a PGND trace.

If you place a PGND layer under the BG trace, the ac-ground return current of the bottom FET will automatically be coupled in a path close to the BG trace. Alternating current will flow to where it finds the minimum loop/impedance. In this case, a separate PGND return trace for the bottom gate driver is not required. It is best to minimize the number of layers on which the gate-driver traces are routed; doing so prevents gate noise from propagating to other layers.

Of all the small-signal traces, current-sensing traces are the most sensitive to noise. The current-sensing signal amplitude is usually less than 100 mV, which is comparable to the noise amplitude. In the LTC3855 example, the Sense$^+$/Sense$^-$ traces should be routed in parallel with minimum spacing (Kelvin sense) to minimize the chance of picking up di/dt-related noise, as Figure 14 shows.

In addition, the filter resistors and capacitor for current-sensing traces should be placed as close to the IC pins as possible. This setup provides the most effective filtering in the event that noise is injected into the long sense lines. If inductor DCR current sensing is used with an R/C network, the DCR sensing resistor, R, should be close to the inductor, while the DCR sensing capacitor, C, should be close to the IC.

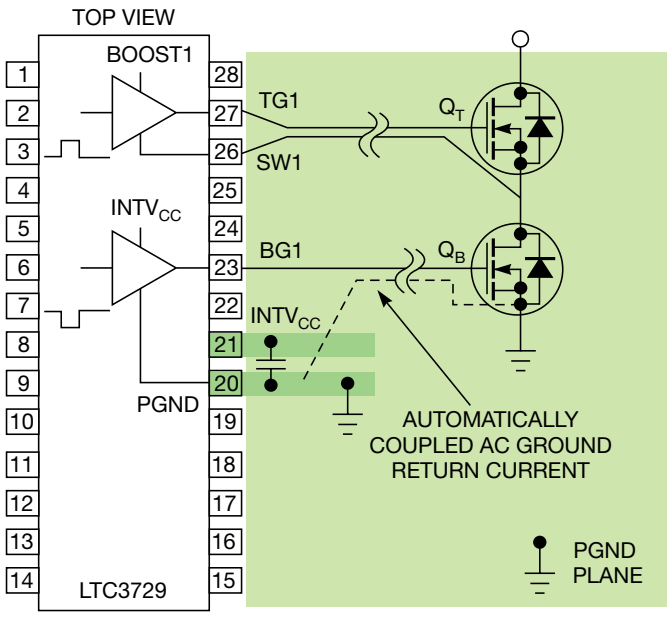


Figure 13 *When routing MOSFET gate-driver traces, using short and wide traces helps minimize impedance in gate-drive paths. The gate-driver current paths should have minimum loop areas.*

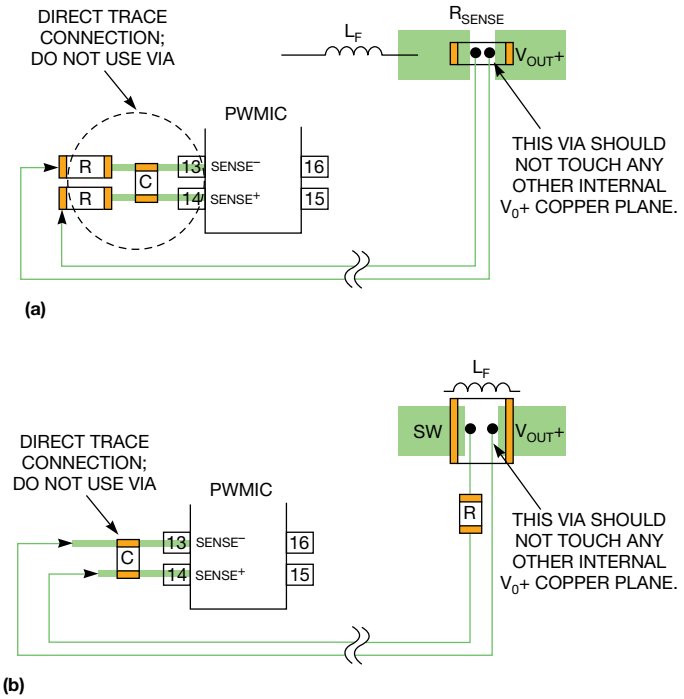


Figure 14 *Kelvin sensing is shown for current sensing, R_{SENSE} (a) and inductor DCR sensing (b).*

If you use a via in the return path of the trace to Sense$^-$, the via should not contact another internal V_{OUT}+ layer. Otherwise, the via may conduct large V_{OUT}+ current, and the resulting voltage drop may distort the current-sensing signal. Avoid routing the current-sensing traces near the noisy switching nodes (TG, BG, SW, and BOOST traces). If possible, place the ground layer between the current-sensing traces and the layer with power-stage traces.

If the controller IC has differential-voltage remote-sensing pins, use separated traces for the positive and negative remote-sensing traces, with Kelvin sense connection as well.

TRACE-WIDTH SELECTION

Current level and noise sensitivity are unique to specific controller pins; therefore, you must select specific trace widths for different signals. In general, the small-signal nets can be narrow and routed with 10- to 15-mil-wide traces. The high-current nets (gate driving, V_{CC}, and PGND) should be routed with short and wide traces. At least a 20-mil width is recommended for these nets.

LAYOUT CHECKLIST

Table 1, available online at http://bit.ly/Ruxanc, provides a sample checklist of the dual-phase LTC3855 supply shown in Figure 10. Using such a checklist will help ensure a well-laid-out power-supply design.EDN

AUTHOR'S BIOGRAPHY

Henry Zhang is an applications engineering manager for power products at Linear Technology Corp. He received his bachelor of science degree in electrical engineering from Zhejiang University in China in 1994 and his master's and doctoral degrees in electrical engineering from Virginia Polytechnic Institute and State University (Blacksburg, VA) in 1998 and 2001, respectively.

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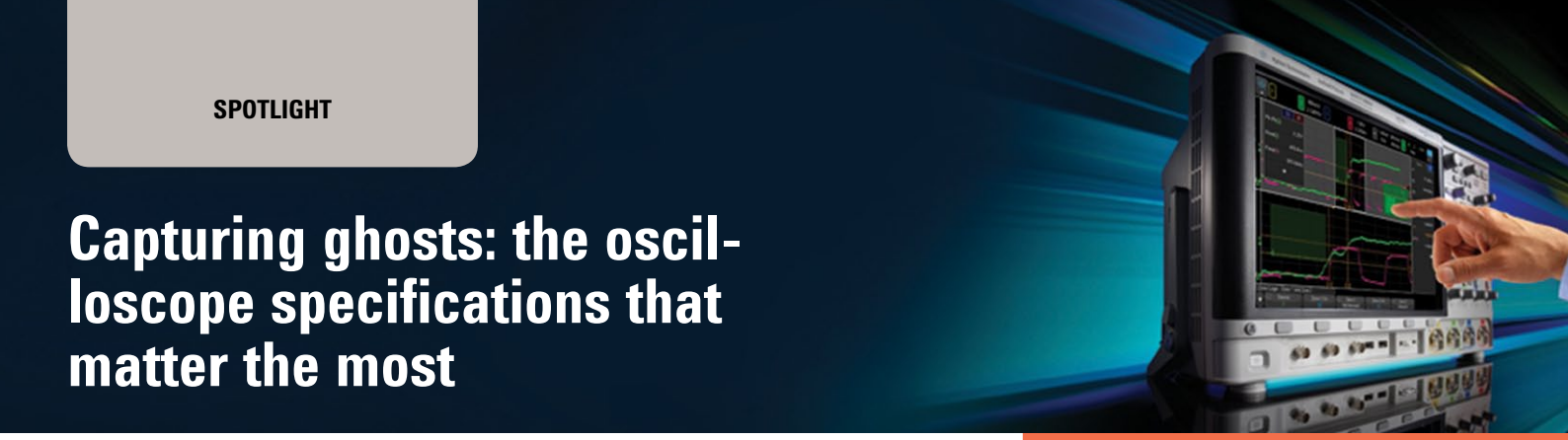
Capturing ghosts: the oscilloscope specifications that matter the most



A flickering "waveform ghost" is a classic intermittent signal—sometimes it's there; sometimes it isn't. A ghost can be an infrequent narrow glitch, an infrequent shift in timing, an infrequent runt pulse, or any inconsistent and unexpected waveform.

These anomalies are among the toughest troubleshooting challenges, so it's vital to understand how scope performance affects your ability to capture, identify, and fix these difficult creatures.

Bandwidth and sample rate

The most important oscilloscope specifications to consider are bandwidth and sample rate. A scope's real-time bandwidth and its associated sample rate determine the level of detail in which signals can be captured. If an infrequent glitch has a very fast transition time or is very narrow, a low bandwidth scope may filter out the glitch entirely, and you'll never know it's there.

Memory depth and display update rate

Deep memory is a powerful tool for catching ghosts because it allows you to sample at higher rates over a longer period of time. However, even if an infrequent event is randomly captured in your scope's deep acquisition memory buffer, will you know it's there? And if you can't readily see it on the scope's display, how do you even know that you need to search for it, or what to search for?

A fast display system greatly enhances a scope's ability to make those occasional waveform ghosts more visible. The higher the waveform update rate, the more likely it will catch and display infrequent anomalies, even when you are not specifically looking for them.

Figure 1 shows an example of a waveform ghost captured on Agilent's new InfiniiVision 4000 X-Series oscilloscope while updating at 1,000,000 waveforms per second. Scopes with slower update rates may never reveal this ghost of a waveform (an infrequent non-monotonic edge).

Assuming that your oscilloscope's update rate is fast enough, the next step is typically to set up the scope to uniquely trigger on it in order to isolate it so that you can determine its root cause. If the infrequent anomaly is a narrow glitch, try using your scope's pulse-width trigger mode. If the infrequent anomaly is a pulse with insufficient amplitude, try using your scope's runt trigger mode. Or if the anomaly is an infrequent non-monotonic edge as in this particular example, try the rise-time trigger mode.

Zone triggering

Chances are you'll encounter situations in which using your scope's advanced parametric/violation triggering modes is easier said than done. A simpler alternative in many cases is zone triggering, which is available on Agilent's InfiniiVision 4000 X-Series oscilloscopes. Simply draw a box (zone) around the area of the waveform ghost using the scope's capacitive touch screen as shown in **Figure 2**, and the scope will display only the anomalous waveforms that intersect that zone.

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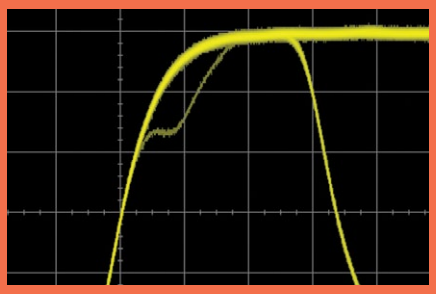

FIGURE 1

The scope's fast waveform update rate reveals an infrequent non-monotonic edge.

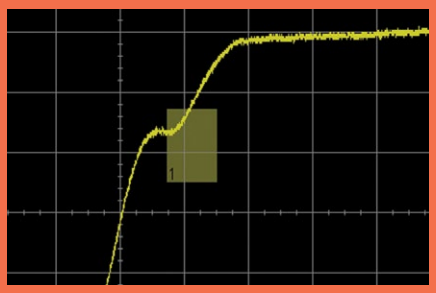

FIGURE 2

InfiniiScan Zone trigger isolates the non-monotonic edge waveform.

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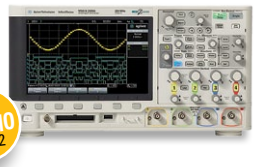

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I2C/SPI trigger/decode		DSOX3EMBD	DSOX4EMBD
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33519B/33521B	30 MHz, 1-Ch (optional arb) / (built-in arb), 30 MHz pulse
33520B/33522B	30 MHz, 2-Ch (optional arb) / (built-in arb), 30 MHz pulse
33210A	10 MHz, 1-Ch, 14-bit, 50 MSa/s, 8 K point (optional arb)
33220A	20 MHz, 1-Ch, 14-bit, 50 MSa/s, 64 K point, 5 MHz pulse
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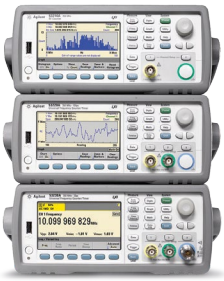

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53220A	350 MHz universal frequency counter/timer, 12 digits/s, 100 ps
53230A	350 MHz universal frequency counter/timer, 12 digits/s, 20 ps

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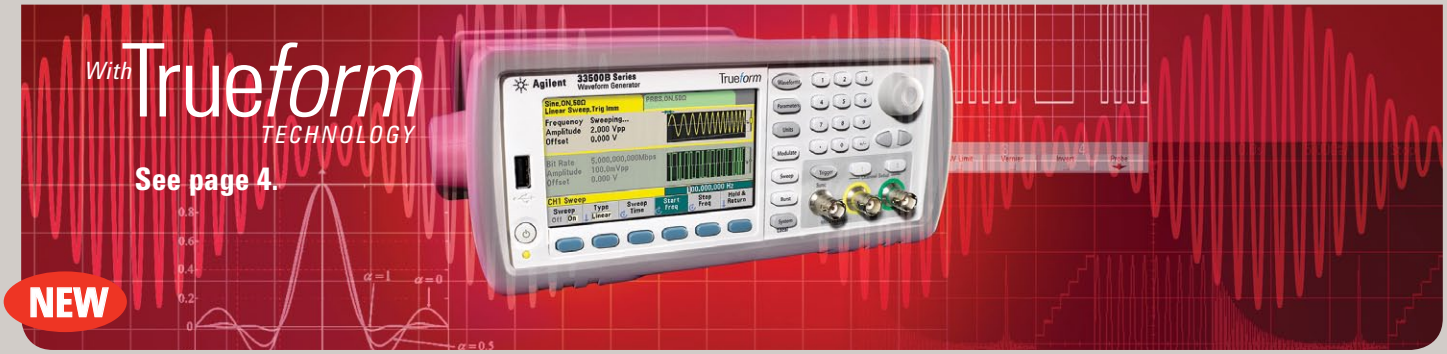

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With these improvements in signal quality and fidelity, the Agilent 33500B Series waveform generators with Trueform are especially useful for the following applications:

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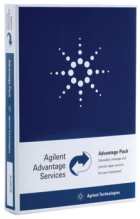

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Published in Spain, February 1, 2013

5991-1539EEE

Anticipate ___Accelerate ___Achieve

Agilent Technologies

BY HOWARD JOHNSON, PHD

Make it better

The circuit in Figure 1 includes a plethora of termination options. The figure shows four results using various combinations of component values, each observed at the point indicated by the purple arrow.

In the first three results, resistor R_2 is replaced with a 0Ω short, and resistor R_3 is not installed. This is a classic series-terminated approach using only resistor R_1, having values of 33, 18, and 4.7Ω, respectively.

Looking at the rising edges, the signal in each case fails to achieve full strength on the first stroke, as indicated by the "plateau" marking on each waveform. In each case, subsequent reflections at 2-nsec intervals push the signal voltage up toward its 3.3V limit. As the value of R_1 is successively reduced, the first stroke becomes more powerful, climbing higher toward the goal of first-incident-wave perfection but never quite achieving it. Even with R_1 set to 0Ω, this driver will never achieve perfection when driving a 50Ω line, because the effective driver output resistance, R_S, is greater than 50Ω.

The falling edges tell a different story. With R_1 set to 33Ω, the initial drop in the falling waveform is 2.7V—a larger step than the first step in the rising waveform. That clue tells us the driver output resistance in the falling direction must be less than the output resistance in the rising direction, a common situation in CMOS totem-pole drivers. In the third waveform, by the time R_1 is set to 4.7Ω, the signal undershoots significantly. The driver in this case is too powerful.

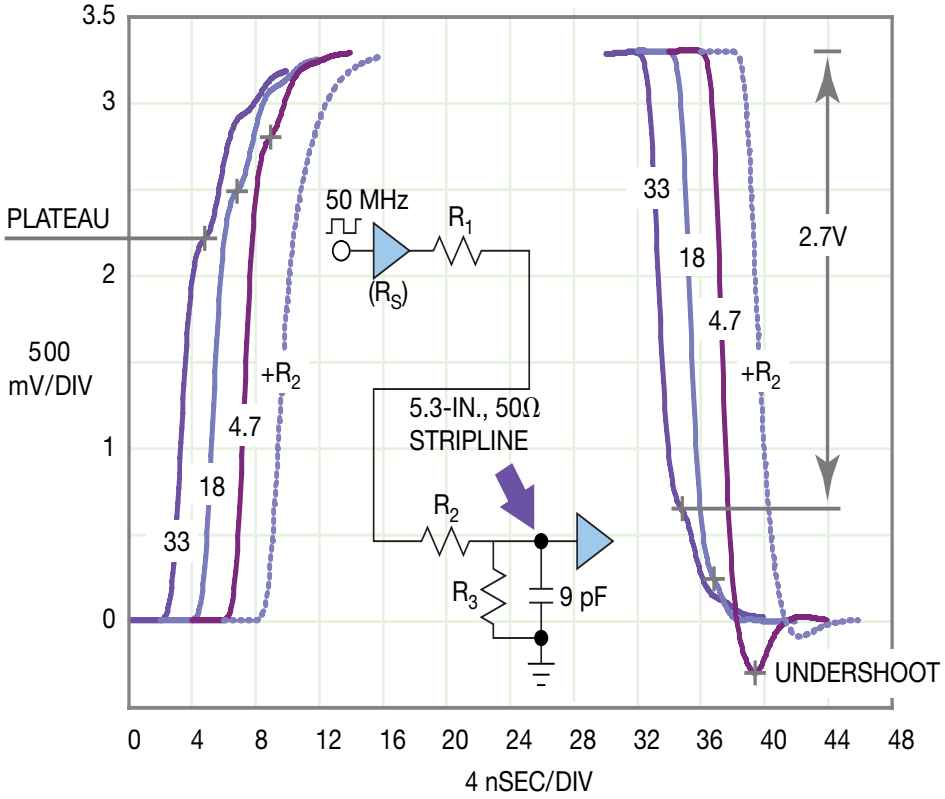


Figure 1 With R_1=4.7Ω, adding R_2=50Ω lengthens the signal-transition times, smoothing the signal and limiting the undershoot.

If your driver output resistance varies between its rising and falling edges, as it often does, then no value of series-terminating impedance can possibly make both edges perfect—but perhaps you can make it better.

A higher value of line impedance helps. To see why, suppose that your driver has output resistances of 60 and 37Ω in the rising and falling directions, respectively, as in this example. Mate that to a transmission line with a characteristic impedance of 10,000Ω using a series resistor of 9,951Ω. The effective impedances in the two driving directions are now 10,011 and 9,988Ω, respectively—very close matches to the line impedance.

Of course, you can't make such a circuit, but even raising your transmission-line impedance to 65Ω permits a higher value of R_1, making R_1 a more significant part of the circuit and thus reducing the impact of variations in the natural output resistance of your driver.

A slower edge helps. The signal rise and fall time now is about 1 nsec. Some FPGA drivers have a facility for slowing the edge-transition time, which would be ideal. If you don't have that, try inserting R_2=50Ω or more in series with the receiver (fourth waveform). That additional resistance, working into the 9-pF capacitance of the receiver, forms a lowpass filter that can lengthen the edge-transition times, reducing the amount of undershoot in the falling direction and making the waveform less sensitive to natural variations in the driver's output impedance. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his website at www.sigcon.com.

POWER

Si vs. GaN vs. SiC

WHICH PROCESS AND SUPPLIER ARE BEST FOR MY DESIGN?

IMAGE: GIULIA FINI

ONE OF THE MOST DIFFICULT TASKS CIRCUIT DESIGNERS FACE IS SELECTING THE OPTIMUM COMPONENTS TO MEET THE DEMANDS OF BOTH THE SYSTEM AND THE ENVIRONMENT.

BY STEVE TARANOVICH • SENIOR TECHNICAL EDITOR

As silicon (Si), gallium-nitride (GaN), and silicon-carbide (SiC) processes are maturing, so, too, are their suppliers' expertise and creativity. It is worthwhile to examine the pros and cons of each process, as well as what is unique about the suppliers of the power elements fabricated on these processes. All of these components factor into the decision on the right solution for a particular design. That solution will be a culmination of process maturity and robustness, as well as supplier expertise, support, and capability—and even some intangibles.

GaN and SiC are wide-bandgap (WBG) materials, which means the energy required for an electron to jump from the top of the valence band to the bottom of the conduction band within the semiconductor is typically larger than one or two electron volts (eV). SiC and GaN semiconductors are also commonly referred to as compound semiconductors, because they comprise multiple elements from the periodic table. Si is a mature incumbent in this arena.

As the race toward leadership in the power element continues to evolve, industry experts have said that by mid-2013 about half a dozen GaN, Si, and SiC suppliers will reveal process enhancements, new architectures, and the latest new capabilities that will bring new choices and tools to the industry. We discuss some of these companies and technologies here.

EFFICIENT POWER CONVERSION

Efficient Power Conversion (EPC) started its GaN efforts five years ago and targeted markets with voltages of 200V and under. The company grows its GaN as an epitaxial layer on silicon.

The two-dimensional electron gas (2DEG) transport mechanism in GaN allows higher mobility of carriers in GaN than in SiC or Si. The 2DEG is on the surface and so lends itself to a lateral device structure; as a result, all of the terminals are located on top of the device.

A problem in existing devices is that the 2DEG in a normally on structure requires a negative voltage on the gate electrode to turn the device off (depletion mode). EPC understood that the power-conversion market would more naturally want to be normally off, so three years ago it developed enhancement-mode GaN (eGaN) devices that are manufactured in the same facility as silicon ICs (Figure 1).

SiC is also used to manufacture power transistors, but because SiC does not have an electron-gas structure, only vertical conduction devices are practical. With a vertical conduction device in GaN or SiC, 1- to 2-kV breakdown voltage levels are easier to reach than with Si. SiC requires an expensive fab, too, because existing Si fab processes are not compatible.

For the future, EPC has plans to go to 900V, which would require a vertical device structure. In that case, SiC has a better thermal conductivity than GaN. GaN, however, has the performance advantage at low voltage and high power and a cost advantage at all voltages. The company predicts the battle between SiC and GaN will begin at the 900V levels and move upward.

AT A GLANCE

- Enhancement-mode gallium nitride (eGaN) is the normally off, natural mode for MOSFETs.
- The primary advantage of silicon-carbide (SiC) MOSFETs is their very low, high-frequency switching losses.
- Silicon (Si) MOSFETs can easily integrate drivers in a single monolithic solution.

In the inverter market for photovoltaic (PV) panels, small to medium-sized inverters with one inverter per panel would ideally fit with EPC's strategy of 900V or less. Higher-voltage devices would fit the central inverter market, which needs to connect a high number of panels together into a big, higher-voltage inverter. This architecture would cause cost and efficiency problems. If one PV panel fails, it would need to be removed from the system to avoid bringing down the entire unit, and efficiency would be lost. If the inverter is trying to convert a lower voltage to the grid-level voltages, however, efficiency would be lost in the inverter itself.

Differences in board space can be seen in a bus converter design for Si and eGaN (Figure 2). GaN transistors are extremely fast. As a result, the system is far more sensitive to the layout than it is with slower Si devices. In particular, stray inductance plays a larger role in the overall system efficiency. Hundreds of picohenries will significantly affect performance.

Stacked devices are better than bond-wire connections. GaN needs no package—it is inert to its environment—and so EPC uses a packageless design. This approach greatly reduces any resistive, inductive, and thermal problems. EPC plans to eventually integrate the driver into the FET.

Episil, EPC's Taiwan-based CMOS foundry, uses 6-in. wafers. EPC plans to scale to 8-in. wafers in the years to come.

The entire process is compatible with silicon except for one machine, which grows the layers of GaN on Si. The metal organic chemical vapor deposition (MOCVD) epitaxial reactor was designed for blue LEDs and is therefore not optimized for eGaN FETs. This is the only step that is more expensive than a straight Si process, so, as the cost of growing epitaxial GaN decreases with improved MOCVD-equipment technology, cost differences compared with Si will become negligible and ultimately disappear.

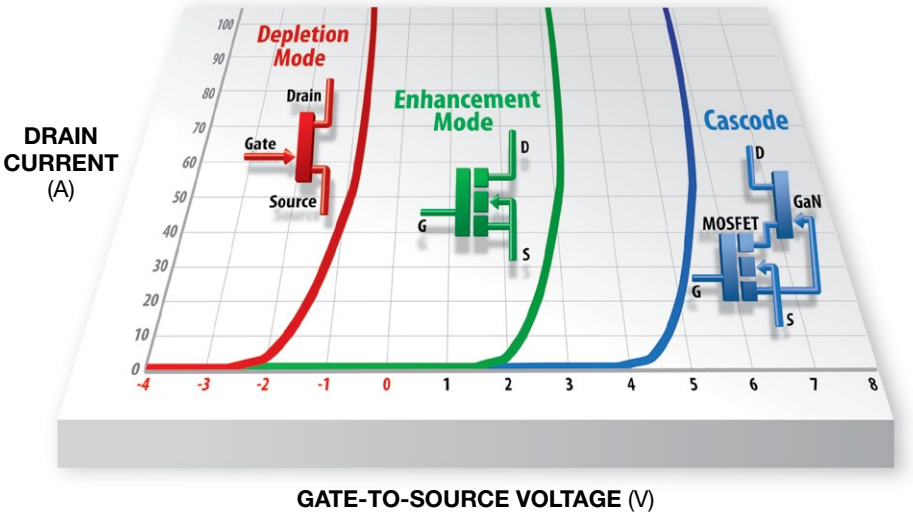


Figure 1 *There are marked differences between eGaN and depletion-mode GaN MOSFETs. Unlike depletion-mode GaN's need for negative voltage turnoff, eGAN requires only positive gate voltages to transition from fully off to fully on.*

GaN SYSTEMS

In speed, temperature, and power handling, GaN is set to displace Si power devices as they reach their performance limits. GaN is the technology that will allow the implementation of essential future "cleantech" innovations, where power, weight, and volumetric efficiency are key requirements.

GaN devices offer five key characteristics: high dielectric strength, high operating temperature, high current density, high switching speed, and low on-resistance (Figure 3). These characteristics flow from its electrical properties, which, when compared with Si, offer 10 times higher electrical breakdown, higher operating temperature, and exceptional carrier mobility.

Taking advantage of these properties, GaN Systems has successfully developed transistors with a key switching figure of merit two orders of magnitude better than that attainable with silicon. This together with GaN's inherent negligible charge storage permits the design of power switching circuits with formerly unheard of efficiencies, small size, and very low heat losses. Using a unique, proprietary, custom "island" transistor topology, the company has overcome the limitation of device operating cur rent associated with traditional "finger" designs. This design approach is applicable to processes that grow a GaN epitaxial layer on base wafers of either SiC or Si. As a result, very low costs can be achieved for fast switches operating at 600V or below built on large-diameter silicon wafers, while operating voltages in excess of 1200V can be achieved using higher-cost SiC base wafers.

At operating voltages below 1200V, the vastly superior mutual conductance afforded by the electron gas that forms the channel of the GaN HEMT is responsible for the devices' two orders of mag-

nitude improved key figure of merit (the product of on-resistance and total gate charge).

SiC gate drives typically require a tightly controlled 20V swing. The island-design GaN devices can be driven with a 5V swing and present significantly lower gate capacitance. GaN-on-Si wafers cost perhaps one-tenth of SiC wafers while having up to four times the area. The GaN Systems island devices also occupy less than half the area of equivalent-performance MOSFET SiC die.

GaN Systems' flip-chip approach to assembly—using copper posts—eliminates the inductance of traditional bond wires. This becomes important with the achievable switching speeds of some 40V per nanosecond. The scalable design topology and the elimination of large switch currents flowing in the on-chip metallization offer the prospect of transistors capable of switching hundreds of amps.

The design also allows packaging approaches for high-power applications that facilitate cooling from both faces of the chip. The GaN switches can be mounted directly onto a custom CMOS driver chip that offers a strong degree of noise immunity and galvanic isolation and can be simply assembled into power subsystem modules.

CREE

Cree is in a unique position in the industry in that it uses a GaN process for its RF devices and an SiC process for its power devices. Due to its in-depth knowledge and use of both processes, the company has made a conscious decision to use SiC for high voltages.

Cree's target market for SiC power devices is 1200V and 1700V solutions, with 600V coming later. At higher voltages, SiC unipolar devices have an advantage over bipolar Si. The challenge at 600V is that Si has better performance, while Si CoolMOS and insulated-gate bipolar transistors (IGBTs) are lower cost.

The primary advantage of SiC MOSFETs is their very low switching losses, which increase efficiency and enable higher-frequency operation. In addition, the SiC MOSFET's positive temperature coefficient allows easy paralleling to obtain higher operating currents.

SiC has been successfully tested at 10-kV levels. Cree targets future MOSFETs at around the 3.3- and 6.5-kV levels and at 10 kV. IGBTs have that market now, but SiC's low switching losses would provide significant performance advantages. Even at frequencies below 4 kHz, SiC MOSFETs substantially reduce losses compared with IGBTs at these voltages.

CREE IS IN A UNIQUE POSITION IN THE INDUSTRY IN THAT IT USES A GaN PROCESS FOR ITS RF DEVICES AND AN SiC PROCESS FOR ITS POWER DEVICES.

Cree's goal is to go to 6-in. wafers from the current 4-in. and a die shrink for high current and 600V to 10 kV over the next few years to lower cost. The company will be able to do this on its existing 4-in. line and convert in situ with no process change. It already has a 6-in. separate LED line. Cree will fill its 4-in. line to capacity and then move to 6 in.—a business decision. The wafers have already been sampled along with 6-in. EPI. All of the company's tools are 6-in.-capable now, and all processes are in-house for SiC.

Avago, Texas Instruments, and Ixys have driver ICs for their products. Cree

feels that good layout and keeping the driver close to the power element will suffice for a good signal without ringing, even though it uses these types of separate Si drivers instead of integrated drivers like an Si MOSFET process can.

As for comparison with IGBTs, SiC MOSFETs' figure of merit at 1200V is less than 20% of switching losses of an IGBT and less than 10% at 1700V. SiC switching losses are much lower than those of IGBTs; the conduction losses are lower, too. Cree's 100A half-bridge module can replace a 200A IGBT and switch at two to three times the frequency with better efficiency (Figure 4).

The company's case as to why SiC can replace Si: SiC is two times better than Si in terms of current and five times better in terms of frequency, with lower thermal losses.

As far as GaN is concerned, Cree has a 6-in. RF line now and is the number 1 supplier in switching. Knowing both SiC and GaN, it chose SiC for power, which is more efficient than Si or GaN. At the same current capability, the company's SiC devices will be smaller than a GaN device.

TEXAS INSTRUMENTS

Early in 2009, TI acquired Ciclon Semiconductor Device Corp, a maker of NexFET MOSFET technology. TI's NexFET power switches are under 30V and synergistic with the company's silicon MOSFET drivers and switching controllers (Figure 5). Having both types of devices on the same process allows for easier integration into a monolithic die containing driver and power elements. This setup eliminates any connection or bonding-wire parasitics that can cause ringing at higher-speed switching between a discrete driver and a power device whether they are on the same or a different process.

Snubbers can be used to reduce ringing, but efficiency would be lost as a result. GaN switching devices certainly have attractive properties, especially above 10 MHz, except for the potential driver/power-device interconnect issues.

Packaging technology is an important part of TI's NexFET solutions, giving them optimal performance. To optimize the performance of a typical voltage regulator, especially for CPUs, you need to minimize the parasitic inductances and resistances in the power circuit formed by the two MOSFETs in the buck power stage. TI accomplished both of these requirements through a unique packaging approach. To achieve a small footprint and the lowest parasitic possible, a stacking topology is used in the NexFET PowerStack package design. PowerStack reduces power consumption by approximately 20% (at 20A) and can reduce device temperatures by more than 30%.

In the GaN arena, TI offers GaN FET driver solutions such as the LM5114, a 7.6A single, low-side driver with independent source and sink outputs, and the LM5113, a 100V integrated half-bridge driver that solves the challenges of driving GaN power FETs. Compared with discrete implementations, these drivers provide significant PCB-area savings to achieve solid power density and efficiency while simplifying the task of reliably driving GaN FETs.

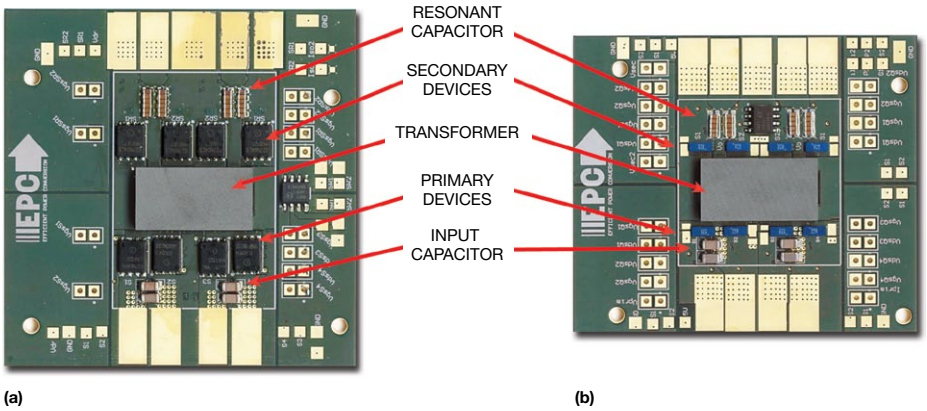


Figure 2 *The experimental bus converter prototypes shown here with V_{IN}=48V and V_{OUT}=12V use an (a) Si MOSFET and (b) eGAN FET in the design.*

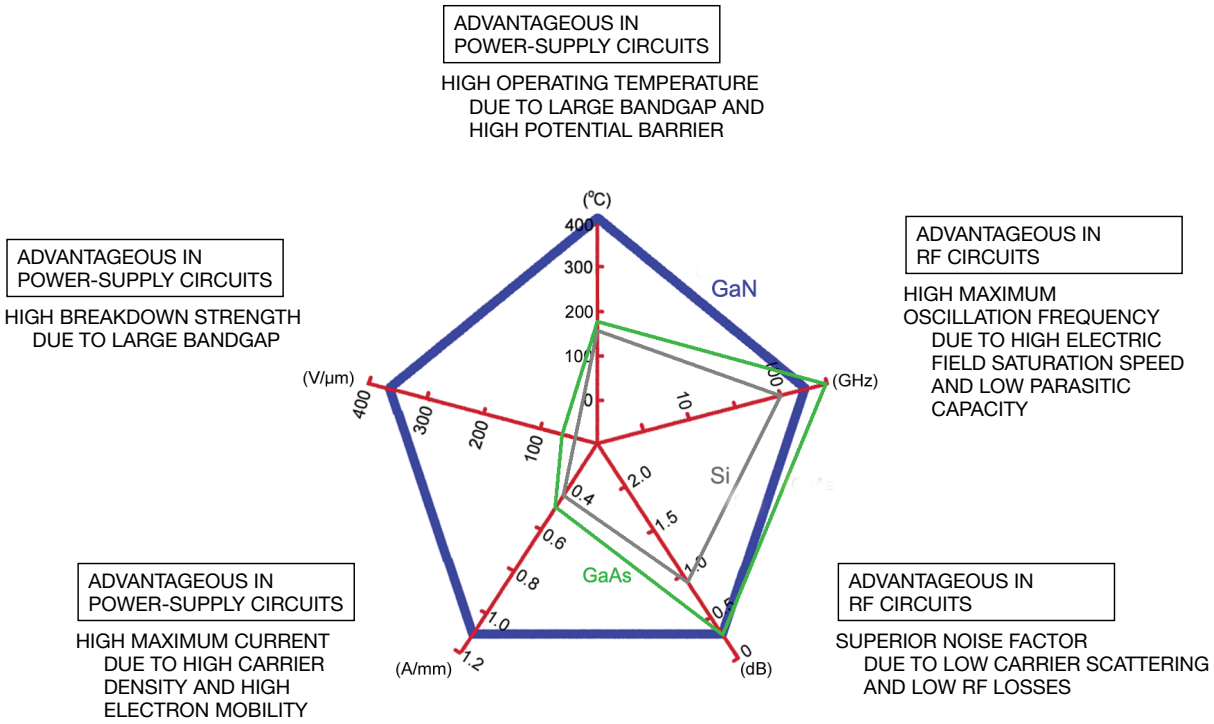


Figure 3 *GaN has five key characteristics, which make it advantageous in power-supply and RF circuits (courtesy GaN Systems).*

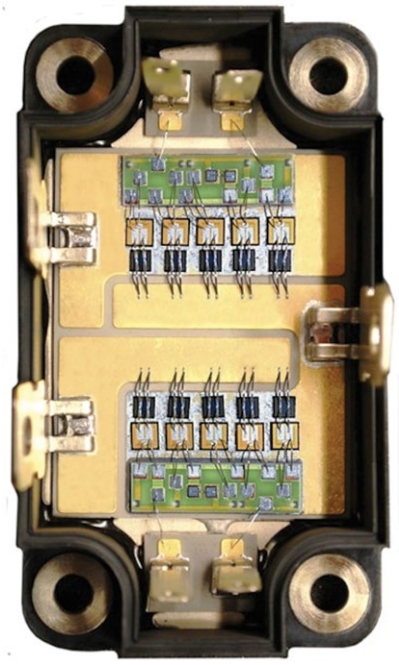


Figure 4 *All-SiC modules can eventually lead to higher integration in one process. The Cree module shown here measures 87.5×50 mm.*

ROHM SEMICONDUCTOR

Rohm Semiconductor's MOSFET manufacturing involves the SiC bulk wafer, epitaxial growth, the power device, and, finally, the integrated power module. With its Japan-based corporate location, Rohm enjoys a solid relationship with the automotive industry. The company also offers a mature SiC Schottky barrier diode (SBD) line. The SiC SBD has 3% to 5% lower forward-voltage drop than Si SBDs.

The SiC MOSFET combines all three key desirable features of the ideal power-element switch (Table 1).

Rohm's MOSFET line, although relatively new, was expected to have a 1700V device in 1Q13 based on second-generation technology. By the end of 2013, the company plans to have packaging higher than its existing temperature devices, which are at 175°C. This allows operation at somewhat lower temperatures than 175°C without a heat sink.

Rohm feels it has the small-package advantage among its competitors, as well as modules that are optimized for performance (Figure 6).

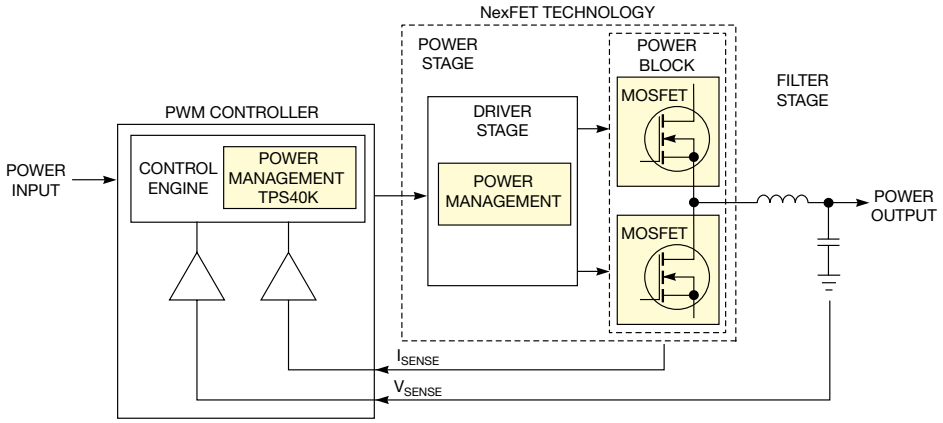


Figure 5 *Texas Instruments' NexFET technology smoothly fits in power-management point-of-load applications.*

MICROSEMI

Microsemi uses the technology customers feel will optimize their designs—Si, SiC, or GaN—from processes performed in-house as well as at outside foundries. It is just getting started with GaN from 40 to 200V for space and high reliability.

GaN is a defect-laden material as compared with SiC and Si, but the company grows GaN on SiC, which minimizes defects. It can reach 1200V on SiC vs. Si and with better efficiency.

Microsemi targets high-temperature applications with its solutions that have the advantages of not needing a heat sink, such as their use in "downhole" applications and in engines where temperature cycling would likely

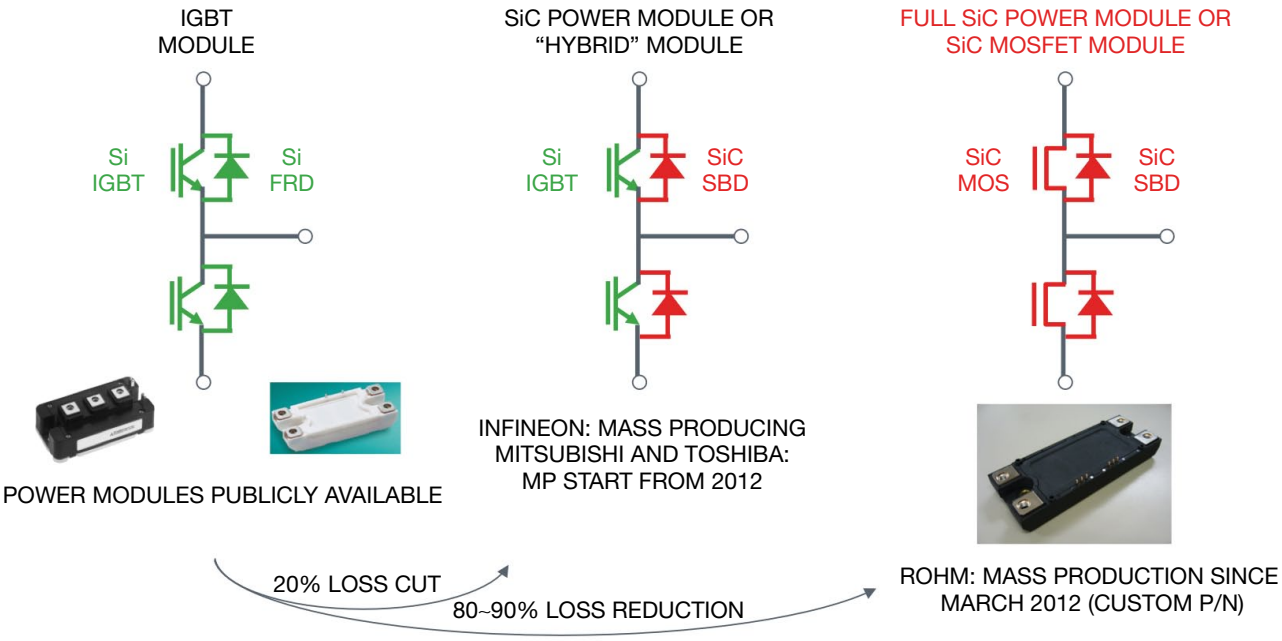


Figure 6 *An all-SiC module greatly reduces power losses by eliminating any Si lossy components (courtesy Rohm Semiconductor).*

cause major mechanical failures with most processes (Figure 7).

INTERNATIONAL RECTIFIER

IR's goal is to target the 20 to 1200V market with better switch on-resistance vs. the V rating of the device to get lower resistance in a smaller package. The figure of merit, based on switch on-resistance, is dramatically improved in the power device, depending on the process and breakdown voltage (see chart below, right). Keeping an eye on a good performance/cost ratio compared with Si is key.

The company believes that GaN on Si is better than SiC to compete with pure-Si devices. It has in-house processes for Si and GaN and also grows its own GaN as well as hetero epitaxial GaN on Si, for which it has IP and patents.

While MOSFET drain-to-source on-resistance is a focus, keeping in mind lower cost, higher efficiency, and better density—or a combination of these characteristics—is also important. GaN devices' value proposition in the power-management chain is evident, as shown in Figure 8.

Class D audio with GaN at higher frequencies gives better noise and harmonic distortion, and the same is true for a power switch.

IR believes that SiC is great at 1500V and above, compared with Si, especially in applications such as electric trains and PV inverters.

A market exists for GaN in automobiles and computer power supplies. IR says early adopters are low-end consumer designs such as class D audio and power supplies, and the design-in time is 18 to 24 months. This is a good near-term market. The five- to seven-year auto- and medical-market cycle is another promising area as the company's product matures.

There are far more selection criteria than what appears in a data sheet or in a simple comparison of Si, GaN, and SiC processes. Consider every aspect of both the supplier and the process, as well as other intangibles, such as experience with and longevity of the process, unique configurations, and synergy with other parts of the system design. Delve deeply into all that is available in this power-element industry that most designers would not consider, and your design will be unique, robust, and the best fit possible for the system's overall needs. EDN

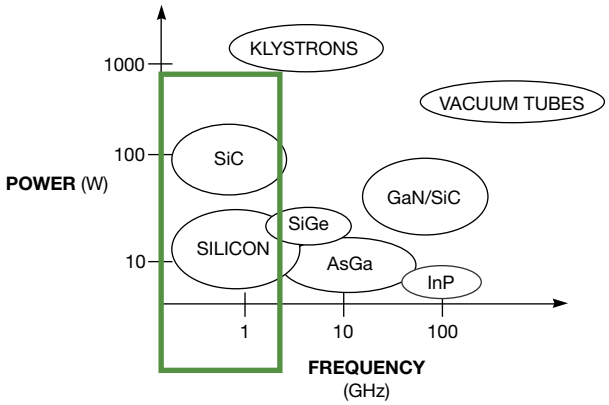


Figure 7 *In this chart showing semiconductor materials and frequency regions, the green box outlines Microsemi's application space.*

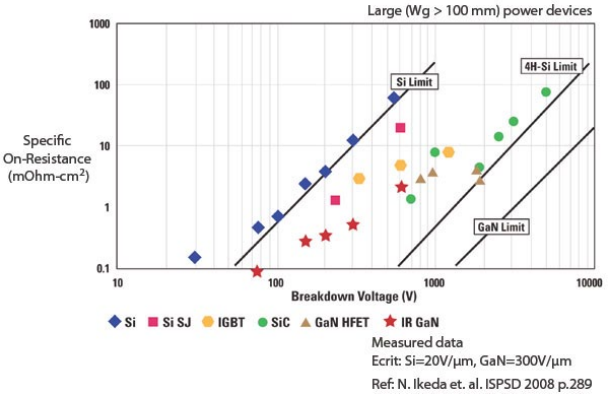


TABLE 1 SWITCHING-DEVICE FEATURES

	SiC MOSFET	Si IGBT	Si Super-junction MOSFET
Breakdown voltage	Up to 1200V currently; higher in the future	High	Up to approximately 900V
On-resistance	Low (only 35% increase from 25°C to 150°C)	Low (but high at lower current due to threshold voltage)	Low (only 250% increase from 25°C to 150°C)
Switching speed	High	Limited switching frequency due to tail current at turn-off <10 kHz	High

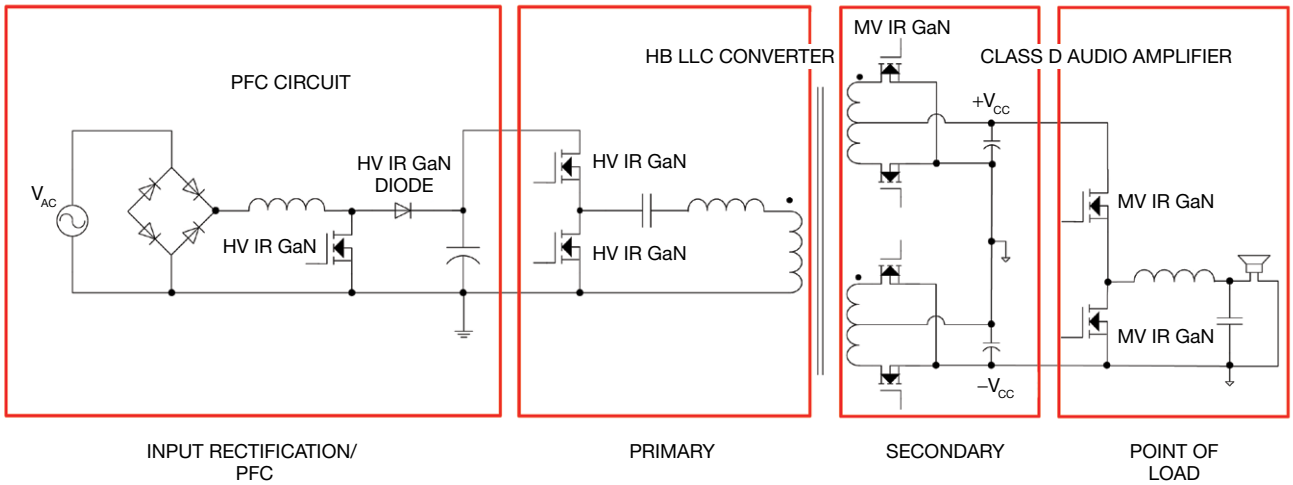
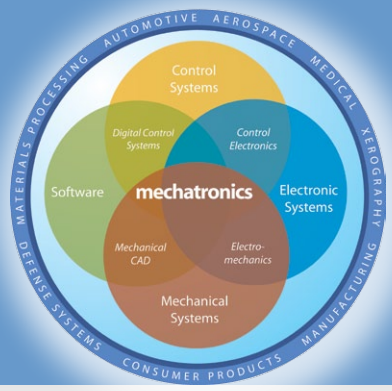


Figure 8 *GaN has a good value proposition in the power-management chain because it can be used throughout the design, adding performance improvements (courtesy IR).*

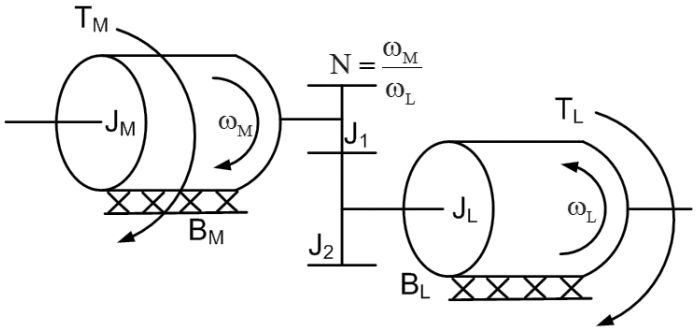


Inertia mismatch: fact or fiction?

Is this often-quoted concept an excuse for inadequate system modeling?

By Kevin C Craig, PhD

Servo systems may be direct drive or geared. For geared systems, the motor selection also involves a choice of gear ratio. Figure 1 shows a motor connected to a load through an ideal (that is, no friction, no backlash, and no compliance) gear train with gear ratio N. The equation of motion for this one-degree-of-freedom system is shown in terms of the load angular velocity, ωL.



$$\left[N^2(J_M + J_1) + (J_L + J_2)\right]\frac{d\omega_L}{dt} + \left[N^2 B_M + B_L\right]\omega_L = NT_M - T_L$$

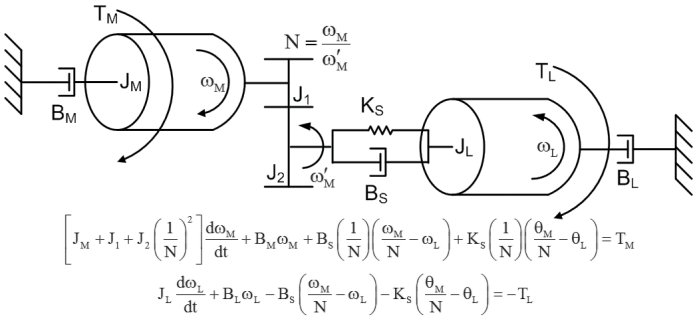
Figure 1 A motor is connected to a load by an ideal gear train.

The inertia ratio is the ratio of the load inertia to the motor inertia, JL/JM. What is the optimum value of this ratio for a particular value of N? If you ignore the motor and load damping, BM and BL, respectively, and the load torque, TL, the inertia ratio that maximizes the power transferred from motor to load is N^2—that is, the reflected motor inertia equals the load inertia.

When friction and load torques and system compliance (for example, coupling or timing-belt compliance) are significant, the selection of an optimum inertia ratio is less straightforward. Figure 2 shows this more general case.

Why do deviations from the so-called ideal inertia ratio of N^2, called inertia mismatch, often cause servo-system stability problems, particularly in compliantly coupled systems? This is a system question, and to answer it you must examine the frequency-response plot for a compliantly coupled motor and load, as shown in Figure 3 (N=1, BM=0, BL=0).

The anti-resonance frequency, ωAR, always occurs before the resonance frequency, ωR. At a low JL/JM ratio, the resonance and anti-resonance frequencies are close to each other at a high frequency. As JL/JM increases, both the anti-resonance and resonance frequencies decrease, with the anti-resonance frequency decreasing at a faster rate. For a given JL, to



$$\left[J_M + J_1 + J_2\left(\frac{1}{N}\right)^2\right]\frac{d\omega_M}{dt} + B_M\omega_M + B_S\left(\frac{1}{N}\right)\left(\frac{\omega_M}{N} - \omega_L\right) + K_S\left(\frac{1}{N}\right)\left(\frac{\theta_M}{N} - \theta_L\right) = T_M$$

$$J_L\frac{d\omega_L}{dt} + B_L\omega_L - B_S\left(\frac{\omega_M}{N} - \omega_L\right) - K_S\left(\frac{\theta_M}{N} - \theta_L\right) = -T_L$$

Figure 2 A motor is connected to a load by an ideal gear train with compliance.

increase the resonance frequency, you need to either increase the shaft stiffness, KS, or decrease the motor inertia. As KS increases, both ωR and ωAR increase. The smaller the inertia ratio, the less the compliance will affect the system.

All mechanical systems have compliance. You should base your choice of inertia ratio and transmission ratio (for example, gear, belt, or lead screw), as well as the design of the feedback-control system, on a system analysis and not on poorly defined rules of thumb. EDN

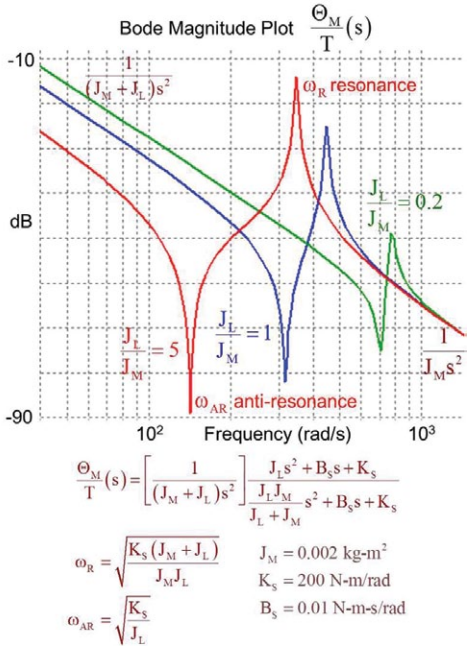


Figure 3 In a compliantly coupled motor and load, the anti-resonance frequency, ω_{AR}, always occurs before the resonance frequency, ω_R.


SPREAD
SPECTRUM
SAFE HAVEN FOR
WIRELESS

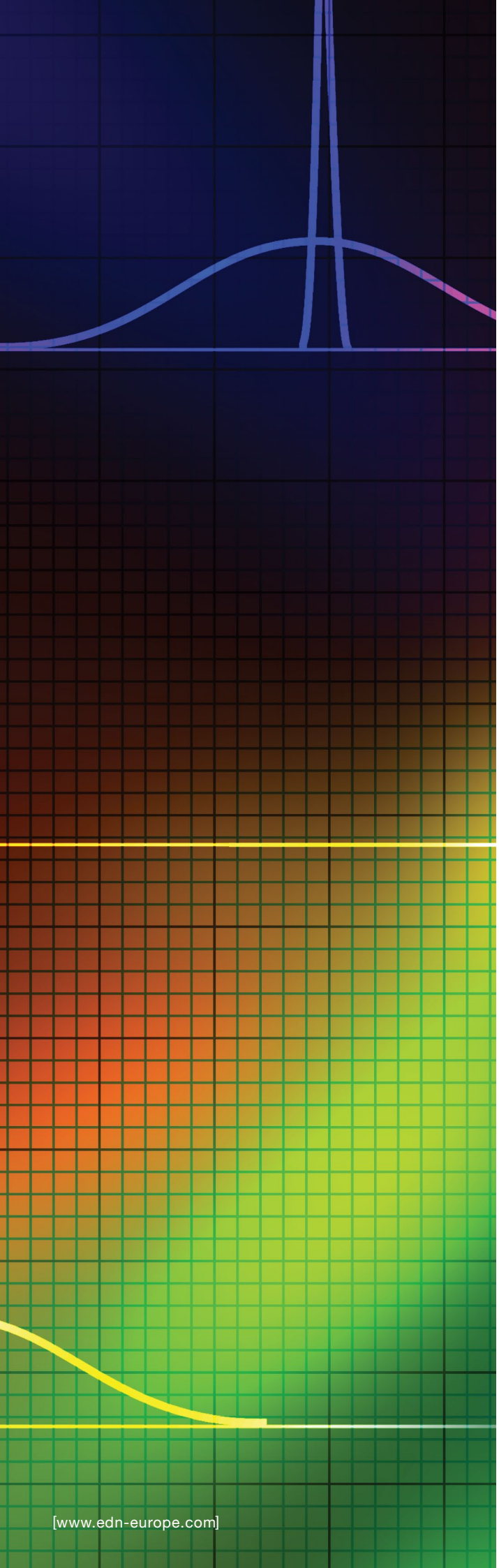


IMAGE: GIULIA FINI

SPECTRUM SPREADING APPEARS TO "WASTE" BANDWIDTH, BUT IT INCREASES CHANNEL CAPACITY, GUARDS DATA SECURITY, AND OFFERS IMMUNITY TO SIGNAL JAMMING AND FADING.

BY RAHUL GARG AND PRAKHAR GOYAL • CYPRESS SEMICONDUCTOR CORP

Wireless communications began to blossom in 1915, with the first wireless voice transmission across the continental United States, and quickly took off from there, with the first commercial radio broadcast in 1920, the first use of police-car dispatch radios in 1921, and the first phone call placed around the world in 1935. Commercial adoption of wireless technology spurred a global radio boom, but the early lack of restrictions on frequency-band usage resulted in noisy channels and unmanageable radio traffic.

The negative impact on communications quality led to the licensing of bands to regulate traffic. Even with legislation, however, further technological enhancements were required to suppress interference.

Moreover, licensing could not be implemented for every band, because reuse of a frequency band is also important for short-range applications. When a channel is used for communication inside a building, for example, its use in a physically distinct location should not be prohibited; such a restriction would result in spectrum underutilization, because such systems will never interfere with one another. Because any number of users could use a license-free band, however, enhancements mitigating interference were even more critical.

Spread-spectrum techniques have been among those enhancements. The concept emerged in the early 1940s and found popularity in

the 1980s as the military embraced its use for data security and intrinsic immunity to signal jamming.

Spread spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum bandwidth necessary to send information. Using spread-spectrum techniques, information contained in a narrow band of frequencies (f_m) is translated, or spread, to a wider band (f_s) before transmission (Figure 1). This translation does not significantly increase the total power required, because the duration of the transmission remains the same; only the frequency changes.

The methods used to achieve spectrum spreading are frequency-hopping spread spectrum (FHSS) and direct-sequence spread spectrum (DSSS). Many wireless communication protocols, such as Bluetooth, use spread-spectrum techniques at the physical-layer level.

WHY SPREAD SPECTRUM?

Though spectrum spreading might appear to "waste" bandwidth, it actually increases the capacity of the channel. The Shannon-Hartley theorem (Equation 1) shows the relationship between channel capacity and channel bandwidth:

$$C=B\times LOG_2\left(1+\frac{S}{N}\right). \quad (1)$$

In the equation, C is the channel capacity, or the maximum number of users that can access the channel simultaneously; B is the channel bandwidth; and S/N is the signal-to-noise ratio.

It is reasonable to assume that the channel-capacity-to-bandwidth ratio in Equation 1 is directly proportional to the required signal-to-noise ratio of the system (Equation 2):

$$\frac{C}{B} \alpha \frac{S}{N}. \quad (2)$$

The relationship, however, is not linear.

For a system with a fixed signal-to-noise-ratio requirement, the only way to increase channel capacity is to increase channel bandwidth. Hence, increasing the number of potential users compensates for the waste of bandwidth. Other advantages of spreading a signal over a larger band include the following:

AT A GLANCE

- Frequency-hopping spread spectrum involves changing the transmission frequency from one subchannel to another. It offers immunity to near-far problems.
- Direct-sequence spread spectrum multiplies each bit of a message signal with a sequence of bits before transmission. The resultant signal is spread over a wider frequency range.
- PN codes in DSSS and the hopping sequence in FHSS both guard against eavesdropping, though a sequence must meet more stringent requirements to qualify as a DSSS PN code.
- The choice of PN codes is critical for the performance of a DSSS system and must exhibit high processing gain, minimal autocorrelation, and minimal cross-correlation.
- Every asynchronous digital communication requires the receiver to synchronize itself with the transmitter. Spread-spectrum systems must synchronize the PN code for DSSS and the frequency-hopping pattern for FHSS.

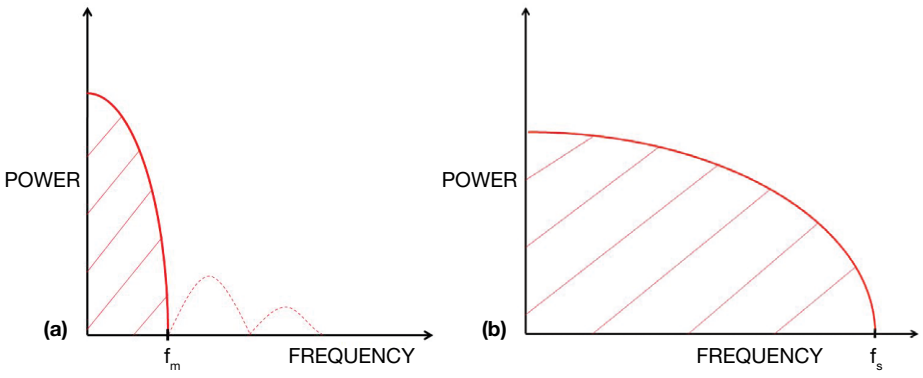


Figure 1 *Using spread-spectrum techniques, information contained in a narrow band of frequencies (f_m) (a) is translated, or spread, to a wider band (f_s) before transmission (b).*

• Anti-jamming. A jammer is a wireless transmitter that continuously transmits to a particular channel with high power. Other co-located devices receive this power as increased noise levels, which prevent them from accessing that channel. If communication occurs in the channel, the entire message signal will be lost. With spread spectrum, only a small part of the signal is blocked.

• Immunity to fading. In wireless systems, it is least likely that the transmitted signal will traverse the same path every time. It may face multiple reflections (or refractions) before actually reaching the receiver.

Those reflections create multiple wave fronts that interfere with one another constructively or destructively. The interference causes distortions or signal-strength reduction (fading) in the received signal. If the fading is significant enough to lower the received-signal-strength (RSS) levels below the minimum required threshold, the receiver cannot successfully decode the signal.

Because fading depends on the physical surroundings of the system, it is modeled as a random phenomenon. Fading, however, has been observed to have dominant effects only for particular frequencies. Hence, spread spectrum offers a measure of immunity because fading will have an effect only on small portions of the signal.

HOW FHSS WORKS

The frequency-hopping spread-spectrum approach changes the transmission frequency from one subchannel to another at regular intervals (Figure 2). A time-averaged view of FHSS requires a much higher bandwidth, even though the instantaneous bandwidth is the same as that of the original message signal.

Hopping among subchannels occurs in a predetermined sequence; thus, each receiver must know the hopping sequence used by the corresponding transmitter in order to remain synchronized. The sequence safeguards against eavesdropping because a receiver cannot successfully decode the message signal without knowing the hopping sequence.

FHSS offers immunity to "near-far problems," or the interference that results when active transmitters are located in proximity to the target receiver. In the absence of FHSS, closely placed foreign transmitters generate a high power level that appears as very high-level noise to a receiver and can blind the receiver if it is communicating in that channel, blocking the communication. With FHSS, the reception bandwidth is bigger; thus, in a worst-case scenario, only some of the hops are blocked, forcing the system to work in less-than-optimum conditions.

HOW DSSS WORKS

Direct-sequence spread spectrum multiplies each bit of a message signal with a sequence of bits before transmission. The resultant signal is spread over a wider frequency range because the chip sequence, also called the pseudo-noise (PN) code, contains multiple-frequency components. The multiplication used here is a logical XOR operation that splits each bit into k number of chips, where k is the length of the PN code (Figure 3).

Because the PN code adds a redundant bit pattern for each bit transmitted, spreading has a direct impact on the effective data rate of the system. For a physical signaling rate of R_P, the effective data rate, R_E, will be given as expressed in Equation 3:

$$R_E = R_P \div n. \quad (3)$$

An increase in the signal's resistance to interference compensates for the reduced data rate. If one or more bits in the pattern are damaged during transmission, the original data can be recovered by processing the redundant bits with a suitable error-correcting method.

Using PN codes, DSSS receivers "tune in" to the corresponding transmitter, tuning out other signals as noise. Because of this selective attention, the signal's resistance to interference increases, and the minimum required signal-to-noise ratio decreases.

Whereas FHSS concentrates the transmitted energy in one subband at a particular time, the energy distribution in DSSS is uniform. DSSS systems transmit over a group of frequencies simultaneously; hence, the range of operation is over wider bands. That uniformity makes the near-far problem more critical for DSSS.

PN codes in DSSS provide security against eavesdroppers, similar to the hopping sequence in FHSS, though in DSSS a sequence must meet more stringent requirements to qualify as a PN code.

DSSS-based systems use a PN-code sequence at the transmitter to spread the narrowband, information-bearing signal into a wideband signal. During transmission, various types of noise and interference affect bandwidth. For proper communication, the corresponding receiver must recover only the desired coded information, rejecting all other signals. Thus, every receiver uses a correlator—a special type of matched filter that responds only to signals encoded with a specific PN code (Figure 4). The DSSS receiver shown in the figure explains concepts related to PN codes.

ERROR CORRECTION

To understand the role of PN codes in error correction, consider a situation in which the incoming sequence and the PN code differ by just one chip. Because the degree of mismatch is low, the correlator output will not be at its peak, but neither will it be at its lowest value. Applying an appropriate threshold limit on the correlator output will allow a receiver to get a rough measure of the degree of mismatch. Based on that measurement, the receiver can make an intelligent decision about whether the incoming sequence corresponds to the desired PN code. PN codes thus provide error correction against corruption of chips.

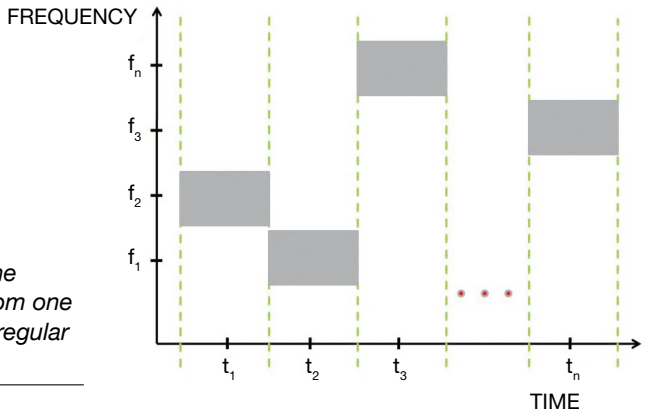


Figure 2 *FHSS changes the transmission frequency from one subchannel to another at regular intervals.*

PN-CODE CHARACTERISTICS

The choice of PN codes is critical for the performance of a DSSS system. PN codes must have certain desired characteristics, including high processing gain, minimal autocorrelation, and minimal cross-correlation.

High processing gain. Processing gain (G_P) is a theoretical system gain that reflects the relative advantage of frequency spreading in terms of channel capacity and immunity against interference. Expressed mathematically in Equation 4, it is the ratio of the chipping frequency (f_c) to the input-signal frequency (f_i):

$$G_P = \frac{f_c}{f_i}. \quad (4)$$

Thus, if a 10-kHz signal is spread over a band of 100 kHz, the corresponding processing gain is 10.

In general, PN codes should add a high processing gain to the system, for two reasons. The first is noise immunity: A higher processing gain implies that the input signal is spread over a larger band that requires the use of longer PN codes. Such systems are more tolerant to noise. The second reason is system capacity. The Shannon-Hartley theorem (Equation 1) holds that channel capacity is directly proportional to the channel bandwidth. Systems with higher processing gain have higher capacity because such systems need a higher bandwidth for transmission.

Minimal autocorrelation. Autocorrelation is the degree of similarity of a signal to its time-shifted version. Equation 5 represents this concept mathematically:

$$R_{AUTO}(\tau) = \sum_{n=0}^{N-1} PN(n) \times PN(n+\tau), \quad (5)$$

where PN(n) is the pseudo-noise sequence, R_{AUTO} is the autocorrelation of the sequence PN(n), n is the length of the PN code, and τ is the delay factor by which PN(n) is shifted.

Time shifting of the signal is not linear; autocorrelation is calculated by shifting it circularly. The autocorrelation is a function of the delay (τ).

For correct decoding, the incoming signal should be phase synchronized with the PN code. The receiver maintains synchronization based on correlator output. Autocorrelation should have a large peaked maximum (Figure 5) for perfect synchronization; that is, τ=0, N, 2N, and so on. Otherwise, there is a high probability that the receiver will be inappropriately phase locked to the incoming sequence. Autocorrelation should be minimal for the slightest mismatch of the two waveforms.

Minimal autocorrelation also provides

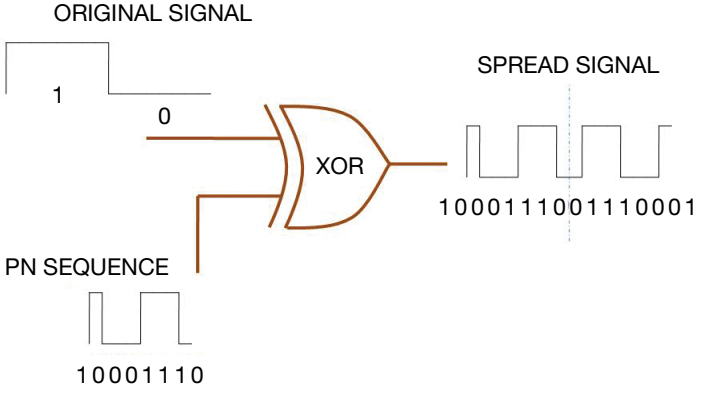


Figure 3 *The multiplication used here is a logical XOR operation that splits each bit into k number of chips, where k is the length of the PN code.*

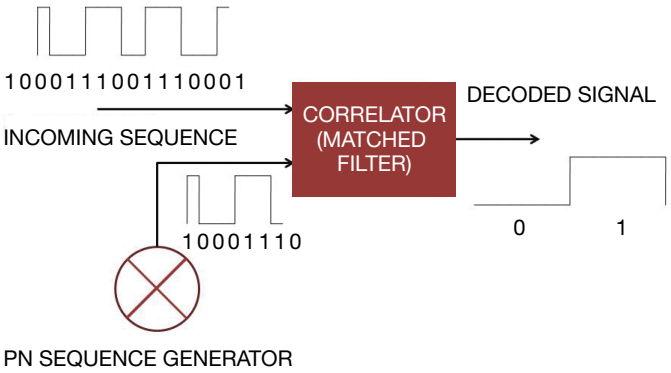


Figure 4 *This DSSS receiver is a functional representation meant to explain concepts related to PN codes.*

enhanced immunity against multipath interference. Once the receiver is phase locked to the incoming signal, it will not actively respond to time-shifted versions of the incoming sequence.

THE INCOMING SIGNAL SHOULD BE PHASE SYNCHRONIZED WITH THE PN CODE. THE RECEIVER MAINTAINS SYNCHRONIZATION BASED ON CORRELATOR OUTPUT.

Minimal cross-correlation. Cross-correlation is similar to autocorrelation but measures the degree of similarity between two independent signals, as is expressed mathematically in Equation 6:

$$R_{CROSS}(\tau)=\sum_{n=0}^{N-1}PN_i(n)\times PN_j(n+\tau), \quad (6)$$

where $PN_i(n)$ is a pseudo-noise sequence; $PN_j(n)$ is another pseudo-noise sequence, completely independent of $PN_i(n)$; R_{CROSS} is the cross-correlation of the sequences $PN_i(n)$ and $PN_j(n)$; n is the length of the PN code; and τ is the delay factor.

Cross-correlation is also called the sliding-dot product. If the cross-correlation between two PN sequences is high, the receiver will not distinguish between the signals encoded over them, because the correlator might have sufficiently high output for both the signals. Here, the receiver might lose "selective attention" capability, resulting in the dominance of interference effects. To minimize the interference from other DSSS sources, different PN codes ideally should be orthogonal; that is, they should exhibit zero cross-correlation.

Because no PN codes are truly orthogonal, choosing the lowest possible cross-correlation mitigates effects.

SELECTING A PN CODE

In general, it is better to have PN codes that provide a high processing gain, but a higher gain requires a larger bandwidth. Another drawback of higher gain is that it typically needs long PN codes, which directly affect the effective data rate of the system. It is also relatively difficult to qualify a long sequence as a PN code because of the higher processing overhead associated with evaluating these characteristics. Due to these factors, selecting an appropriate PN code is a tedious task.

To simplify the process, some standard codes—Gold codes, m-sequences, and Walsh codes, for example—are chosen as a candidate for PN codes. These codes are known to have desirable characteristics; for example, m-sequences have low auto-correlation, while Gold codes exhibit low cross-correlation properties.

A typical approach for selecting PN codes is to choose some sequences from these standard codes and rate them separately on all of the desired characteristics (usually autocorrelation and cross-correlation only). These sequences can be ranked, based on the assigned ratings and application requirements. The ranks can then be used for deciding whether the corresponding sequence is fit to be a PN code.

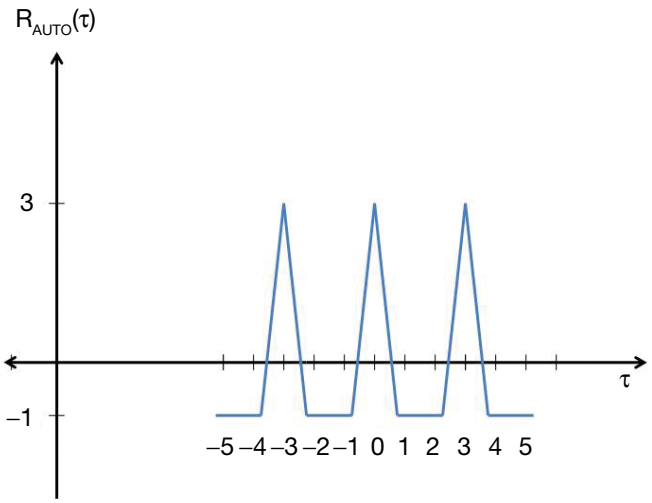


Figure 5 *Autocorrelation should have a large peaked maximum for perfect synchronization only; otherwise, there is a high probability that the receiver will be inappropriately phase locked to the incoming sequence.*

Once an appropriate spreading method and spreading sequence are chosen, the next critical step is to establish synchronization between a transmitter and the corresponding receiver. Every asynchronous digital communication requires the receiver to employ a mechanism to synchronize itself with the transmitter; otherwise, it would be impossible for the receiver to decode the incoming signal. Because they are asynchronous in nature, spread-spectrum systems must synchronize the PN code for DSSS and the frequency-hopping pattern for FHSS.

Synchronization is established in two phases: acquisition and tracking. In the acquisition phase, the receiver detects whether the incoming signal is from the desired source. In the tracking phase, the receiver performs fine synchronization and tracks the incoming signal in terms of phase, frequency, or both, using a locking mechanism.

SYNCHRONIZATION IN DSSS

With DSSS, if the correlator output is less than a minimum threshold, it will discard the incoming sequence as background noise. Because the autocorrelation of a PN code is minimal, the correlator output is very low—ideally, zero—if the incoming sequence and the locally generated PN code are not phase synchronized. Without explicit measures for synchronization, the receiver could not decode the incoming signal reliably.

Because the PN code achieves signal spreading in DSSS, the carrier frequency of the transmitter remains the same, and there is no need for frequency synchronization between the transmitter and the receiver.

ACQUISITION IN DSSS

Correlation between the incoming sequence and the locally generated one has a peaked maximum for perfect synchronization. Using "serial" or "parallel" search, the receiver searches for a phase in which the correlation exceeds a predefined threshold.

In serial search, a monitoring circuit keeps check on correlator output. If the output fails to reach a threshold value, then the search-control block shifts the phase of the generated PN code (Figure 6). This process repeats until the correlator output reaches the threshold value, completing acquisition. The configuration forms a feedback loop, referred to as a sliding correlator.

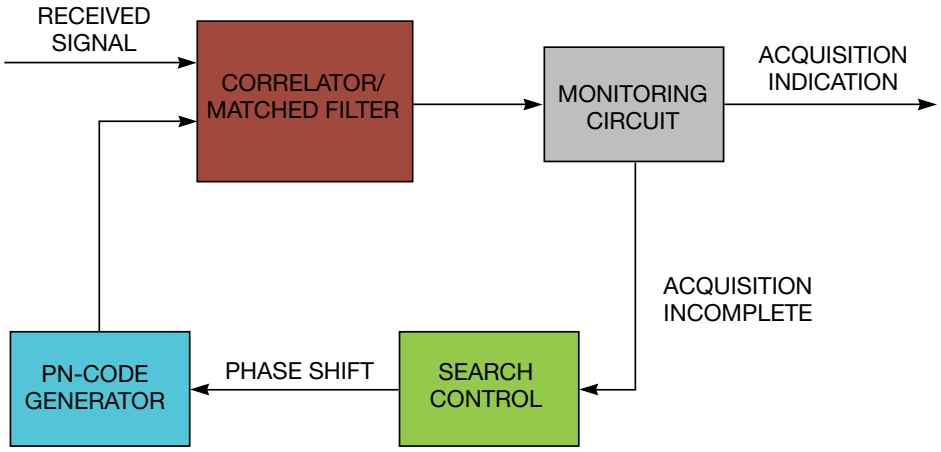


Figure 6 *In serial search, a monitoring circuit keeps check on the correlator output. If the output fails to reach a threshold value, the search-control block shifts the phase of the generated PN code.*

One potential drawback to serial search is that acquisition times are high. Hence, some designs use a parallel approach.

A parallel-search strategy is essentially the same as serial search, but it shortens the acquisition time because it carries out multiple phase comparisons simultaneously, albeit at a trade-off of increased hardware-resource requirements and complexity. The acquisition time is the lowest with a parallel strategy when the number of correlators equals the number of chips in the PN code.

The acquisition process achieves only a coarse synchronization. The degree of synchronization achieved at the end of this phase is within $\pm T_C/2$, where T_C is the chip duration.

TRACKING IN DSSS

Once acquisition is complete, the receiver starts tracking the phase of the incoming sequence to achieve finer synchronization. A delay-locked loop (DLL) is commonly used (Figure 7). The DLL generates three phases, or versions, of the PN code—the delayed, advanced, and precise phases—and continuously compares the output of the correlator using the delayed PN code and the output using the advanced PN code. This comparison provides a measure of the direction of phase drift in the incoming signal; using this metric, the phase of the precise version of the PN code is dynamically adjusted.

The precisely phased PN code remains accurate throughout the reception process. It is this version of the PN code that is used for the actual despreading of the received signal (Figure 7).

SYNCHRONIZATION IN FHSS

With FHSS, because the transmitter keeps changing the center frequency, the receiver and the corresponding transmitter should be in the same frequency channel. Another important requirement is that both transmitter and receiver should spend the same amount of time in a particular channel; otherwise, the receiver might hop to another channel prematurely and lose synchronization with the transmitter.

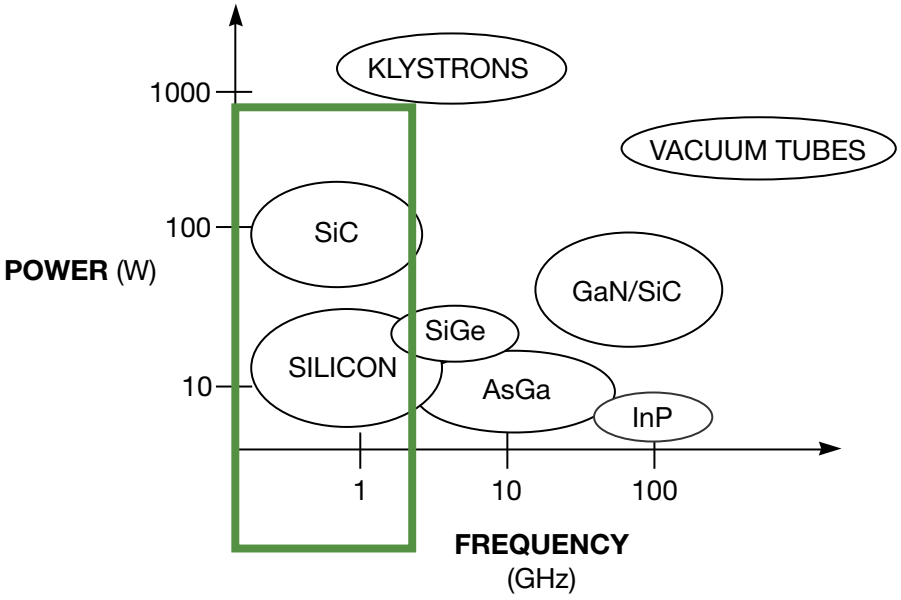


Figure 7 *Given that dynamic adjustment is a continuous process, the precisely phased PN code remains precise throughout the reception process. It is this precise version of the PN code that is used for the actual despreading of the received signal.*

ACQUISITION IN FHSS

Acquisition in frequency-hopping systems refers to frequency synchronization; its purpose is to put the receiver and transmitter on the same frequency channel. The simplest approach is a dedicated acquisition channel wherein the transmitter and the receiver must initiate communication on the dedicated channel only and wait until acquisition is complete. If the dedicated channel is jammed because of noise, communication will not occur.

Another approach is to start hopping at power-on. The transmitter's hopping rate should be faster than that of the receiver to ensure that the devices end up on the same channel.

TRACKING IN FHSS

After acquisition, the receiver should be able to track the transmitter. Both the transmitter and the receiver should stay in a channel for the same duration and hop to the same new channel once that period is over. Timing synchronization is easier to implement in FHSS than in DSSS because the hopping rate is fixed for both devices. To determine the next channel, the devices have a preloaded lookup table containing available channel numbers.

SYSTEM PERFORMANCE

The synchronization process needs a certain amount of delay for both DSSS and FHSS. Hence, most protocols have an additional header for the sync pulses to ensure that the receiver and the transmitter are synchronized before packets with meaningful information are transmitted. EDN

AUTHORS' BIOGRAPHIES

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Circuit maximizes pulse-width-modulated DAC throughput

Ajoy Raman, B , India

Simple DACs realized by low-pass filtering microcontroller-generated pulse-width-modulated (PWM) signals have a response that is typically a tenth of the PWM frequency. This Design Idea is a novel implementation of a previously published method[1] employing a reference ramp whose output is sampled and held by the PWM signal. This approach results in a throughput rate equal to the PWM frequency.

You can use the circuit in Figure 1 to implement a ±10V 10-bit DAC with a throughput of 20 kHz. A DSPIC30F4011 microcontroller (not shown) is operated at a clock frequency of 96 MHz to generate the capture signals OC_1 and OC_4. Clock/4 is fed to an internal 16-bit timer whose period is set for a count of 1200 corresponding to a PWM frequency of 20 kHz. Signal OC_4 is mostly high and goes low at a fixed count of 1170 as a reference for ramp generation. IC_{1A}, along with Q_1, forms a precision constant-current source that linearly charges capacitor C_2 when Q_2 is off. This signal inverted by IC_{3A} switches Q_2 on for a period of 30 counts to discharge C_2 for the start of the next ramp. IC_{1B} buffers, amplifies, and offsets the ramp; potentiometers R_2 and R_5 adjust the offset and gain.

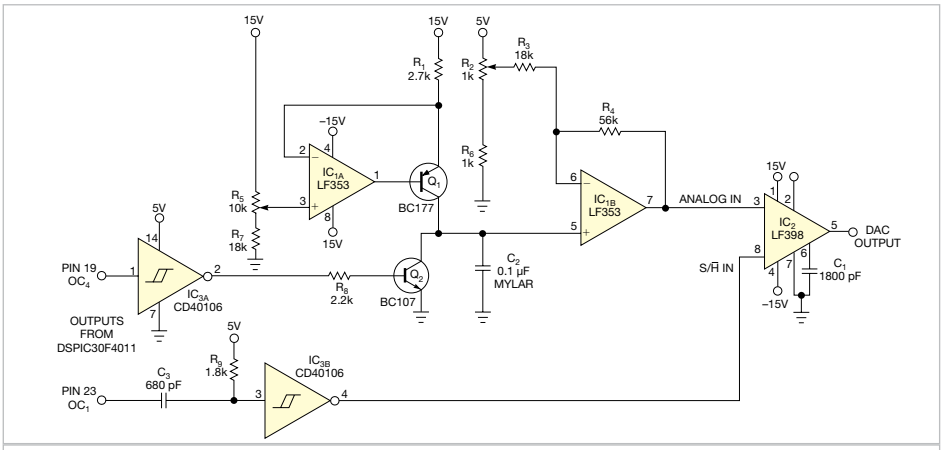

Figure 1 The off-page microcontroller generates signals for ramp control (OC_4) and sample timing (OC_1).

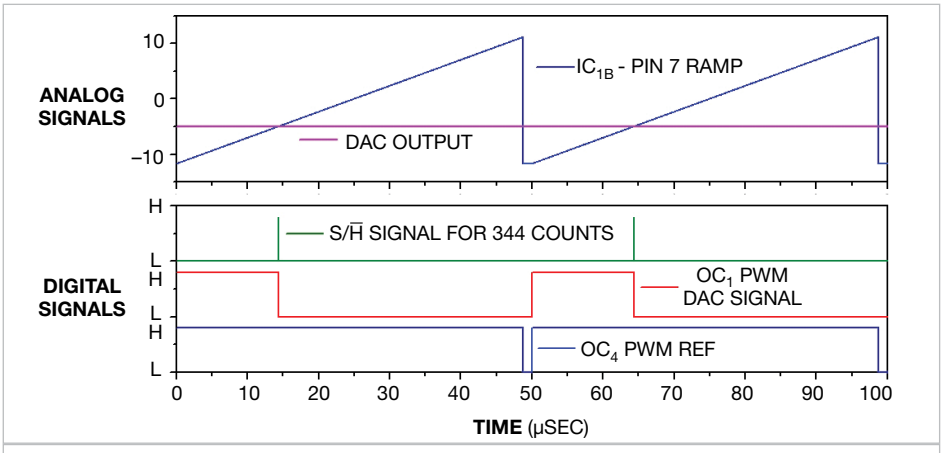

Figure 2 The differentiated OC_1 falling edge generates the S/$\overline{H}$ sample pulse at the ramp −5V point.

The OC_1 falling edge controls the PWM DAC sample timing relative to the ramp voltage. The data word to be converted determines the OC_1 duty cycle by comparing it internally in the microcontroller with the internal 16-bit timer. C_3 and R_9 differentiate the resulting PWM signal; IC_{3B} then inverts it, forming a 1-µsec sample signal for the sample-and-hold IC_2. Pin 5 of IC_2 forms the DAC output and is adjusted to −10, 0, and +10V for OC_1 PWM counts of 88, 600, and 1112, respectively, corresponding to a 10-bit count of 1024.

The count offset of 88 helps to avoid the initial nonlinear region of the ramp so that the PWM DAC shows good linearity with a LSB of 20 mV and an accuracy of ±40 mV. Additional PWM DACs could also be implemented using capture PWM outputs OC_2 and OC_3.

Figure 2 shows the waveforms to be expected for a DAC output corresponding to 256 on a 10-bit scale of 1024. OC_4 forms the PWM reference based on which a 20-kHz bipolar ramp signal is output at Pin 7 of IC_{1B}. This ramp is sampled and held at a count of 256+88=344, corresponding to a DAC output of −5V.EDN

DIs Inside

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A circuit for mains synchronization has two separate outputs for each half-period

Dušan Ponikvar, University of Ljubljana, Ljubljana, Slovenia

Often a measurement of weak signals has to be performed in the presence of strong interference from the ac power mains. If the interfering signal cannot be filtered out, then you can still obtain a clean result by making two consecutive measurements separated in time by an odd number of half-periods of the mains and calculating the average of the two measurements. The interfering signals have opposite polarities in consecutive measurements, and averaging cancels them out. If you average several consecutive pairs of measurements, the results will improve still further. Instead of counting the half-periods of the mains, you may find that a circuit having two outputs for synchronization with odd or even half-periods of the mains can come in handy.

The circuit shown in Figure 1 provides two separate and optically isolated outputs, ISO_1 and ISO_2, for synchronization with the desired half-period of the mains. Figure 2 shows the results of simulation (using the free version of TINA-TI). The circuit accepts mains input from 80V ac to 240V ac, and consumes under 1 mA.

THE CIRCUIT ACCEPTS MAINS INPUT FROM 80V AC TO 240V AC.

The duration of the pulses at outputs ISO_1 and ISO_2 is less than a millisecond, and capacitor C_1 can be adjusted to achieve the exact alignment of the falling edges of outputs ISO_1 and ISO_2 with the zero crossing of the mains. All diodes, D_1 to D_5, are small-signal type 1N4148 or similar.

The circuit works as follows: During the positive half-period of the mains, C_3 is charged through R_{1A}, R_{1B}, D_1 and D_5, D_3, R_{2B}, and R_{2A}. The effective time constant, τ, for charging is about 43 msec, and C_3 barely picks up some charge in the half-period. Once the mains drops below the voltage stored on C_3 (this happens just before the end of the half-period), the charging stops and current begins to flow from C_3 through R_3 into the base of Q_5, turning it on. This discharges C_3 through the LED in optocoupler OC_1, and produces a pulse at the output ISO_1 of the circuit. During the negative half-period, the action repeats, only this time D_4 and D_2 are used to charge C_2, and R_4 is used to activate Q_5 when the negative half-period is nearly finished.

The duration of the output pulse can be shortened to about 600 µsec by increasing the time constant—therefore by increasing the value of resistors R_1 and R_2 or capacitors C_2 and C_3—but this also reduces the range of acceptable input voltages.

The detailed simulation reveals that the maximum voltage on C_2 and C_3 is less than 5V, with 250V ac connected to the input; a voltage rating of 10V for the capacitors is sufficient. Additionally, the maximum voltage on C_1 is less than 10V ac, and the reverse voltage on the diodes is less than 6V. The peak current through the optocoupler LEDs is below 8 mA. The only components that are exposed to the mains are input resistors R_{1A}, R_{1B}, R_{2B}, and R_{2B}. They have equal values, so each one needs to withstand 25% of the mains voltage.

The measurements obtained from the constructed circuit show good correlation with the simulation results. Figure 3 shows output signals; Figure 4 shows the timing detail of the zero crossing and corresponding output pulse for three different values of C_1.EDN

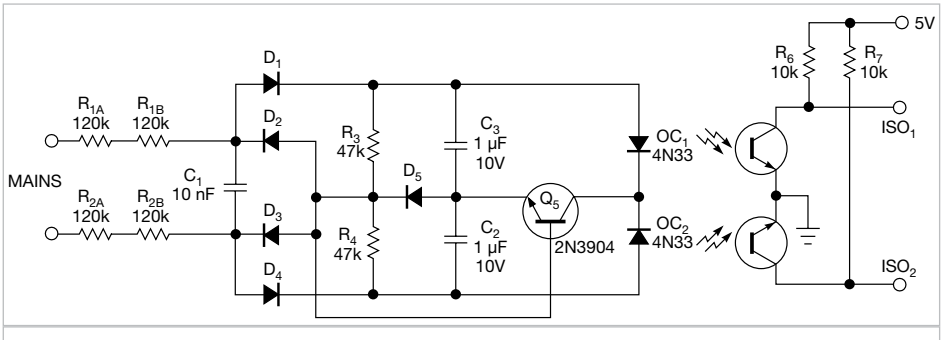

Figure 1 Mains zero crossings are marked by the optically isolated outputs.

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1. "DIY: Isolated high-quality mains voltage zero-crossing detector," www.dextrel.net/diyzerocrosser.htm.
2. Matteini, Luca, "Mains-driven zero-crossing detector uses only a few high-voltage parts," EDN, Dec 1, 2011, www.edn.com/4368740.

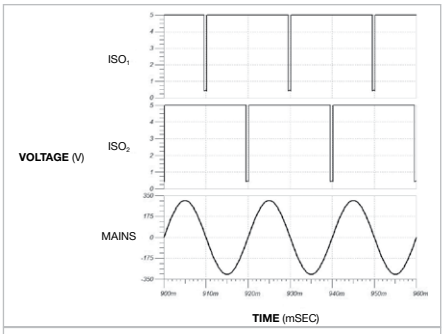


Figure 2 Simulation results demonstrate the circuit action.

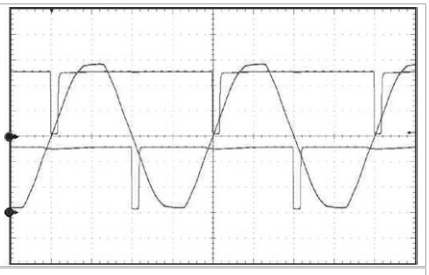


Figure 3 Measured output signals ISO_1 and ISO_2 and the mains voltage verify the circuit operation.

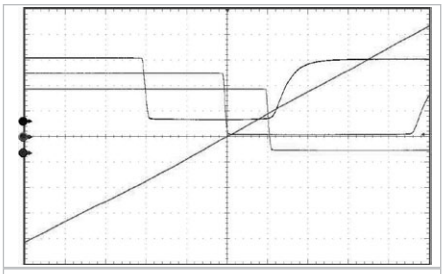


Figure 4 C_1 determines the position of the pulse leading edge in this detail from the center portion of Figure 3. The horizontal scale is 200 µsec/div. Pulses are vertically shifted for better visibility: C_1=0 (upper), 12 nF (middle), and 22 nF (lower).

DC-DC converter starts up and operates from a single photocell

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The bq25504 from Texas Instruments is a good candidate to become a milestone on the road to micro-power management and energy harvesting. A prominent feature of this IC is its ability to start up at a supply voltage as low as 330 mV typically, and 450 mV guaranteed. With an SMD inductor and a few capacitors and resistors, it forms a dc-dc converter with a high power efficiency that is unprecedented, especially in the ultralow-power region.

A possible explanation for this breakthrough in achieving an extremely low value of start-up voltage could be the use of an internal oscillator based on submicron-wide-channel FET transistors. It is known that the narrower the FET's channel is, the lower its threshold value of gate-source voltage will be—down to a few hundred millivolts. You could assume that FETs in the internal oscillator of the bq25504 have a threshold voltage on the order of 200 mV.

The circuit in Figure 1 differs from those shown in the bq25504 data sheet (www.ti.com/product/bq25504) in that it exploits a feature of the bq25504: The reference voltage at V_{BAT_OV} (overvoltage) is internally multiplied by a factor of 3/2, as compared with the reference voltage at V_{BAT_UV} (undervoltage). If limiting the battery voltage within an interval of V_{BAT_UV} and $(3/2)\times V_{BAT\_UV}$ suits your application, you can connect the V_{BAT_UV} and V_{BAT_OV} inputs as shown in the figure and use a single resistor divider network for both, instead of two separate divider networks.

Thus, not only do you save two resistors, but you also can lower the value of the sum of resistances as $R_{UV1}+R_{UV2}=5M$ without sacrificing the overall power efficiency of the circuit. As a by-product, you get a higher insensitivity to EMI at the V_{BAT_UV} and V_{BAT_OV} inputs.

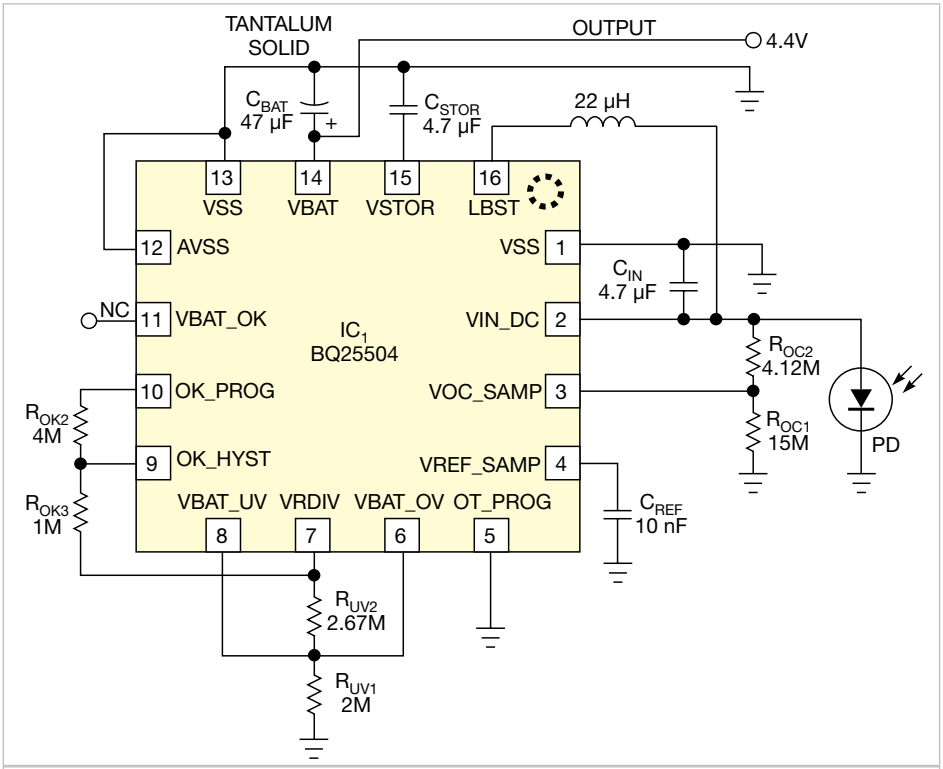


Figure 1 By exploiting the inherent weights of V_{BAT_UV} and V_{BAT_OV} inputs as 2/3:1, you can save at least two precision resistors in many applications. (IC_1 is shown from the bottom view since, if breadboarding, the package style requires connections from the bottom.)

The bq25504 has an ability to draw the maximum possible power from an input source. A photovoltaic cell, due to its nonlinear nature, outputs maximum power at about 80% of its open-circuit voltage. Resistors R_{OC1} and R_{OC2} determine this operating point of the solar cell, PD. This novel IC even tracks the chosen source operation point slowly to get as much power as possible under varying input source capability.

Experiments were performed with a single solar cell of diameter D=7.5 cm positioned horizontally on a desk located 1 meter from a window. Although it was sunny outside, practically no direct sunlight passed through the window. Under these circumstances, the short-circuit current, I_{SH}, of the solar cell was 16.27 mA. Note that the I_{SH} of the same cell reaches a value of 300 mA when the plane of the cell is oriented perpendicularly to full-sun radiation. With no load on the converter, the output voltages V_{BAT} and V_{STOR} varied from 4.396V to 4.404V. This ±0.1% variation can be attributed to the fact that the boost converter operates in discontinuous mode to compensate for self-discharge of the capacitors C_{BAT} and C_{STOR} and then idles for a relatively long time. The solar-cell terminal voltage was 0.441V with the converter unloaded.

When a 10-kΩ load resistor was connected to the V_{BAT} output, this "wavering" of V_{BAT} and V_{STOR} disappeared, and both become a constant 4.4V. The dc component of V_{IN_DC} dropped to 0.4073V. By increasingly shadowing the solar cell with a metallic plate and thus depleting the energy available, I was able to reach an operating point where the output voltage was still 4.4V, while the mean value of voltage at the photocell terminals had dropped to 0.336V. It can be assumed that at this point the converter had entered a continuous-operation mode. (Note that even though the bq25504 data sheet shows V_{STOR} as the loaded output, in this application V_{BAT} is used as the output because even a low output voltage is often better than none under energy-deficient conditions.)EDN

Filter quashes 60-Hz interference

Adolfo A Garcia, Analog Devices, Santa Clara, CA

The circuit in Figure 1 filters 60-Hz interference from low-frequency, low-level signals. The filter exhibits 40-dB rejection (Q=0.75) and draws 95 µA max from a single-sided 5V supply.

IF ADDITIONAL REJECTION IS NEEDED, CASCADE FILTER SECTIONS.

Resistors R_1, R_2, and R_3 and capacitors C_1, C_2, and C_3 form a classic twin-T section, and IC_1 and IC_2 provide local and global feedback. The frequency selectivity (Q) and the rejection performance of this active filter are very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Table 1 shows rejection and Q as a function of the value of R_Q.

R_4, R_5, C_4, and IC_3 form a very-low-impedance reference source to bias IC_1 and the twin-T section to half the supply voltage.

To configure the filter to operate at 60 Hz, choose a Q that will provide enough rejection without excessive loss of desired low-frequency signals that may be close to the filter's notch frequency. The value of R_Q is expressed as

$$R_Q=(4Q-2)R_7.$$

The gain of the output amplifier is simply that of a conventional noninverting amplifier:

$$A=1+(R_Q/R_7)=4Q-1,$$

and the overall gain of the band-reject filter below and above the notch frequency is expressed as

$$V_{OUT}/V_{IN}=2A/(1+A).$$

If you need additional rejection, cascade filter sections. Keep in mind that you might have to modify the circuit to account for out-of-band gain multiplication.EDN

TABLE 1 R_Q REJECTION AT 60 Hz, AND THE FILTER'S VOLTAGE GAIN AS A FUNCTION OF THE FILTER Q

Filter Q	R_Q (kΩ)	Rejection (dB)	V_{OUT}/V_{IN}
0.75	1	40	1.33
1	2	35	1.5
1.25	3	30	1.6
2.5	8	25	1.8
5	18	20	1.9
10	38	15	1.95

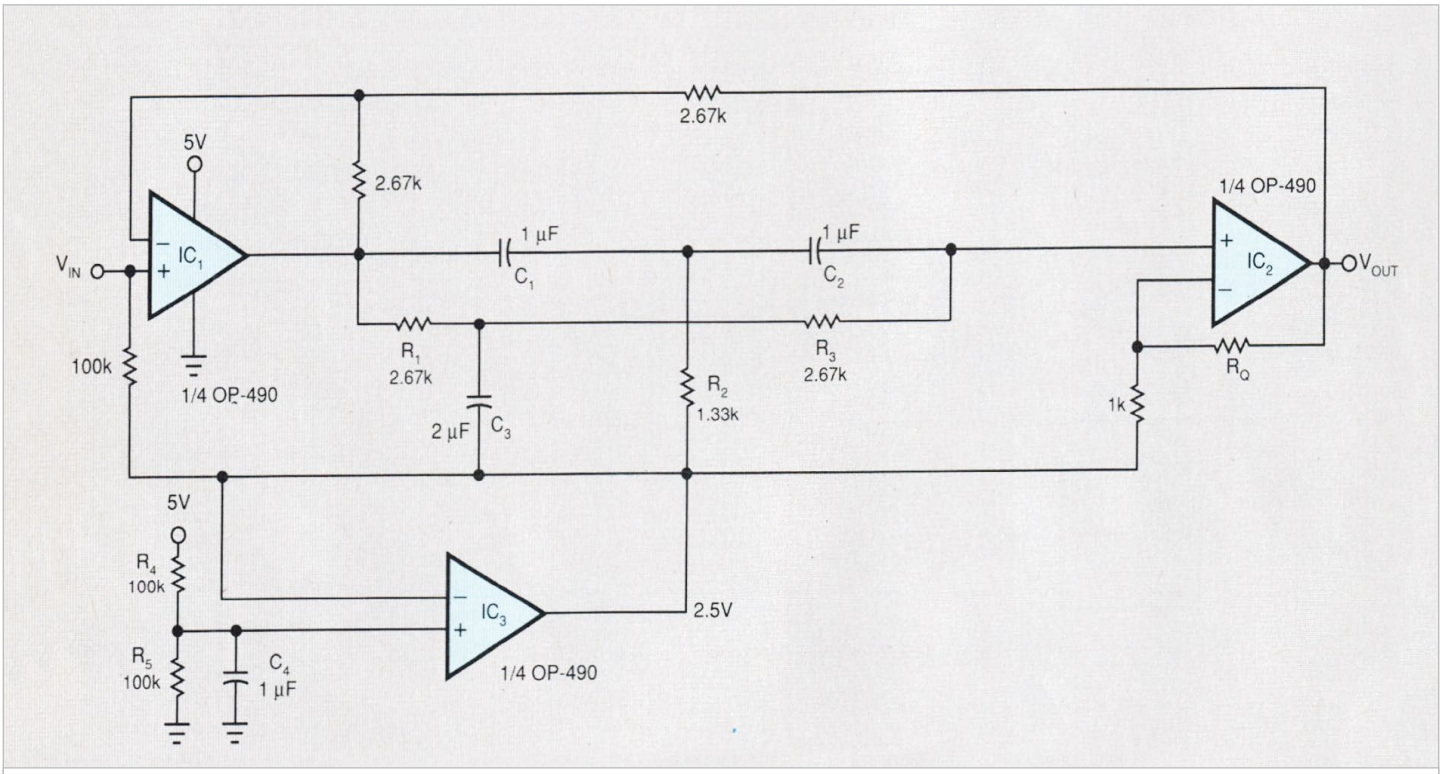
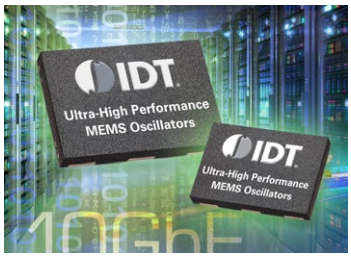


Figure 1 This notch filter suppresses 60-Hz interference in low-frequency signals.

productroundup

USB signal generators offer popular bands to 4 GHz

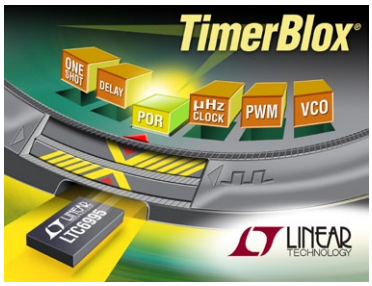
Vaunix Technology, manufacturer of Lab Brick USB powered test equipment, has announced eight new models in its LMS Series of signal generators covering 70-450 MHz, 250-1500 MHz, 600-3200 MHz, and 1000-4000 MHz. The Lab Brick LMS series of USB-compatible, synthesised signal generators features low noise, fast 100-µsec switching time, and fine 100 Hz frequency resolution, requiring no additional DC supply voltage. Advanced features include phase-continuous linear-frequency sweeping; selectable internal/external 10 MHz reference; optional pulse modulation; ability for GUI software to track and control several connected signal generators, simplifying multiple-signal test setups; and device storage of settings in internal memory, allowing it to power up in a specific instrument state. The new models include: LMS-451D, a 70-450 MHz unit with +10, +13, and +20 dBm output power options; LMS-152D, a 250-1500 MHz unit with +10, +13, and +20 dBm output power options; LMS-322D, a 600-3200 MHz unit with +10 dBm output power; and LMS-402D-13, a 1000-4000 MHz unit with +13 dBm output power.



Vaunix; http://vaunix.com/products/lms-signal-generator/overview.cfm

Low frequency clock IC generates long intervals

Linear Technology's LTC6995 is a simple, accurate low frequency clock configurable for long duration power-on reset and watchdog timer applications. The LTC6995 is the latest part in the TimerBlox family of versatile silicon timing devices, which combines an accurate programmable oscillator with precision circuitry and logic. A wide resistor-settable frequency range provides a clock period from 1msec to 9.5 hours. Upon power-on or a reset signal, the LTC6995 will initiate a full output clock cycle. The reset capability and programmable period are specifically intended for long duration timing events. The LTC6995 is simply programmed, using 1 to 3 resistors, with a maximum frequency error guaranteed less than 1.5%. The reset function will truncate the output pulse, clear the internal dividers and hold the output in a high or low state. The polarity of the reset input and the output signal can be configured for active-low or active-high operation. Two versions of the LTC6995 are available, with inverted reset functionality; the reset on the LTC6995-1 is active high, and active low for the LTC6995-2. The output polarity in the reset condition is selectable for both versions. LTC6995 costs $1.35 (1,000)



Linear Technology, www.linear.com/product/LTC6995

Microchip increases analogue and I/O resources in 16-bit MCU family

Microchip has extended its 16-bit PIC microcontroller family with analog integration and configurable low pin-count options for cost-sensitive automotive, consumer, medical and industrial applications. The PIC24F "KM" family provides a new level of integrated analogue functionality such as a 12-bit ADC with threshold detection, 8-bit DACs for analogue control loops and precision comparator references, as well as op amps to assist in sensor amplifications. The KM MCUs are the first to feature the new Multiple-output Capture Compare PWM Module (MCCP) and Single-output Capture Compare PWM Module (SCCP) peripherals, which include integrated timers and advanced PWM control to enable motor-control, power-supply and lighting applications. The MCCP and SCCP modules combine timers, input captures, output compare and PWM functions in a single time-base for optimal flexibility. This is also the first PIC24 family to offer a Configurable Logic Cell (CLC) for increased on-chip interconnection of peripherals. The CLC module helps in creating custom real-time logic functions on-chip and is supported by the CLC configuration tool, which helps in coding the circuit graphically instead of in assembly or C, thereby saving time for the programmers. The PIC24F "KM" MCUs operate from 1.8 to 3.6V, while PIC24FV "KM" versions operate from 2 to 5.5V.

Microchip, www.microchip.com/get/B7SP

Single module provides ovened crystal, GPS, time and frequency reference

Incorporating the SmarTiming+ GPS/GNSS disciplining software operating at 1-nsec resolution, the GXClok-500 reduces the price point for the next generation of high-performance timing applications. Designed with a highly adaptable architecture, the GXClok-500 features a small footprint of 76 x 20 x 38 mm, 50-channel GPS/GNSS receiver, high frequency accuracy when locked to GPS of ±3E-12, and high frequency stability over a wide temperature range option of ±3E-10 over -40°C to +85°C. Other characteristics include low aging of ±1E-10/day, high long-term frequency stability of 2E-8/year, and low phase noise of -95 dBc/Hz at 1 Hz from the 10 MHz carrier. Power consumption is 3 W nominal, short-term stability is 1E-11 at 1 second, and warm up takes 7 minutes. High holdover options when unlocked to GPS/GNSS of 10 µsec/24 hours and low g-sensitivity options of 5E-10/g are available. The makers says that integrating a high precision OCXO crystal oscillator and a flexible GPS/GNSS receiver in a 3.6 inch cube volume makes it an attractive product for many cross industry applications.

Spectratime, www.spectratime.com

More memory and GPIOs for MSP430 MCUs

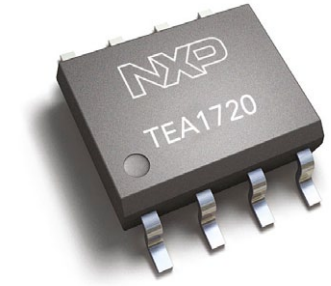
New MSP430G2xx4 and G2xx5 devices from Texas Instruments enable wireless and advanced capacitive touch capabilities with additional serial ports, timers and die-sized packages. TI has grown the MSP430 Value Line microcontroller series with new G2xx4 and G2xx5 devices. These new devices offer memory from 16 kB up to 56 kB Flash and up to 4 kB SRAM, enabling you to migrate existing solutions and support connectivity

protocols such as wireless MBUS and near field communications (NFC). By combining the increased memory resources and integrated capacitive touch IOs on the MSP430G2xx5 devices, you can implement more sophisticated capacitive touch capabilities such as swipe, gesturing, double tap and proximity effects within their applications. Up to 50% greater code density compared to standard 8-bit microcontrollers is possible, TI says. Standby power is 1µA and fast wake-up time of < 1µsec gives low-power consumption. Integrated intelligent peripherals, such as 10-bit analogue-to-digital converters (ADCs), UART, comparator and serial communication, offload CPU tasks for increased power efficiency. You can also add reliable high bit-rate serial communications to designs with the G2xx4 and G2xx5 microcontrollers' high-frequency crystal input; high frequency, low parts per million (PPM) external crystals achieve <0.1% clock source accuracy. MSP430G2xx4 and G2xx5 microcontrollers are priced from $0.96/$1.12 (10,000), sampling now. The MSP430 LaunchPad expansion board will be available in May for $15. The MSP-TS430DA38 target board and MSP-FET430U38 Flash emulation tool are both immediately available from TI's eStore for $75 and $149, respectively.

TI; www.ti.com/mspvalue-g2xx-pr-lp

GreenChip power IC family offers mobile charging benefits

NXP Semiconductors has introduced its latest GreenChip designed to make portable device chargers more compact, energy-efficient and cost-effective – without sacrificing reliability. Used together, the GreenChip TEA1720A and TEA1705



are high-performance, low-power controllers for mobile device chargers up to 10-W. The latest GreenChip solution introduces an architecture that uses the secondary side (TEA1705) for load-step detection, generating wake-up interrupts to the primary side (TEA1720A) in burst mode. The TEA1720A is the primary sensing SMPS (switched mode power supply) controller driving an external bipolar transistor, while the TEA1705 functions as the secondary-side transient controller. Together, the TEA1720A and TEA1705 deliver a fast transient response (5V ±5%). This approach supports the use of smaller output capacitors – 2 x 270 µF or lower – which, combined with the high integration level of the overall GreenChip solution, reduces the PCB space required and enables chargers in a compact form factor of about 1 inch^3. It also enables low no-load power consumption of less than 10 mW.

NXP, www.nxp.com/pip/TEA1720A4T and www.nxp.com/pip/TEA1705

Aluminium electrolytics upgraded

Panasonic's FR Series of aluminium electrolytic capacitors is designed for applications that require ultra-low ESR, an extended product life, and are tight on space. The FR-Series has up to 30% increased capacitance over Panasonic's current comparable product, the FM series.

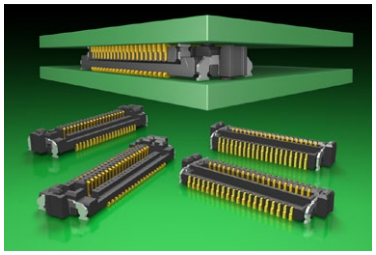
In addition, the FR Series has up to 100% longer product life (up to 10,000hours at 105ºC). They have a rated voltage range of 6.3V – 63V and a capacitance range of 4.7µF – 8200µF. FR aluminium electrolytic capacitors are small and compact, measuring only 5(diameter) x11mm - 16 x 25mm. Suitable applications include adapter and power supply switching, LCD backlights, LED applications and devices requiring an extended product life.

The Panasonic V-ZA Series is a conductive speciality hybrid capacitor which combines the low ESR characteristics of speciality polymer capacitors and the advantage of low leakage current. Compact in design, they also offer the high reliability advantage of speciality polymers and the safety of aluminium electrolytic capacitors. Technical specifications include: a capacitance range of 10µF - 330µF; a temperature range between -55ºC and +105ºC, a rated voltage range of 25VDC to 80VDC. Suitable applications include telecommunication base stations, switching power supplies, DC/DC converters, automotive equipment, industrial electronics, smart meters and many others.

Panasonic from TTI; http://ttieurope.com/page/panasonic-microsite

Low-profile connector system increases stacking density

Samtec's line of Razor Beam interconnects now includes an ultra low profile, micro pitch system for high speed performance in space saving applications. Razor Beam LP low profile



socket and terminal strips (SSH/STH Series) achieve a low 2.00 mm stack height with surface mount termination to the board: 2.50 mm and 3.00 mm stack heights are currently in design. This 0.50 mm (.0197") pitch interconnect system features contacts designed for micro pitch and low profile interfaces. The system features a double row, slim body design for increased PCB board space savings with 20, 40, and 60 total pin counts: 80 and 100 total pin counts are in development. Weld tabs are optional for easy board processing as well as for more rugged applications. The range also includes a low profile, ultra-fine 0.40 mm (.0157") pitch system (SS4/ST4 Series) with stack heights from 4.00 mm to 6.00 mm. The socket and terminal strips feature up to 100 positions on a double row, extra narrow body design for PCB real estate savings.

Razor Beam interconnects include micro rugged hermaphroditic interfaces for high speed/high density applications. These self-mating systems reduce inventory costs and are available in a variety of pitches and lead styles for increased flexibility. The slim row-to-row design is available on 0.50 mm (.0197") pitch (LSHM Series), .250" (0.635 mm) pitch (LSS Series) and 0.80 mm (.0315") pitch (LSEM Series) systems for parallel, perpendicular and coplanar applications.

Samtec; www.samtec.com

BRUCE BUSHEY • TEST ENGINEER

Rush-project troubleshooting comes down to the wire

In 1981, I needed a less expensive method for connecting ICs than the standard etched-copper PCB. I was looking for a method that would produce circuits faster than prototype PCB fabrication and that would allow many changes to be made quickly at low cost. I chose wire wrap, which was used a lot in that decade of digital circuits.

The wire-wrap process uses a motorized tool that wraps a small-gauge (30 AWG) wire tightly around each square IC socket post. The four square corners on the socket posts dig into the wire to provide a low-resistance electrical path. Little did I realize the troubleshooting problems that lurked ahead when I chose this manufacturing method.

The rush was on to wire a dozen board types for a prototype and production system. We chose a universal board with 12 rows of 100 wire-wrap pins. The 100 pins allowed the use of five DIP ICs with 20 leads, seven 14-pin ICs, or any combination not exceeding 100 pins.

Two technicians wired all of the boards using the wire-wrap method. With today's electronic cross-checking tools, we have come to expect 100% of our boards to work 100% of the time. Thirty years ago, we were getting only half the boards to work the first time.

To troubleshoot the faulty wire-wrap boards, we used a good board and traced the clock and other signals from the origination to the next IC. Was too much capacitance loading down the clock oscillation?

We did not have the problem Tracy Kidder describes in his book The Soul of a New Machine. Kidder relates a story in which short pieces of wire-wrap wire broke off, shorting various points together. Initial wraps might have been perfect, but when the unwrapped wires were used again, it was common for a half-inch piece of wire at the end to break off and fall into the maze of pins and wires, creating electrical havoc.

In our case, the oscillator ran on the faulty board, but the rest of the board did not function. To troubleshoot, we used a Tektronix 455 scope, putting the amplitude control on the variable setting and then looking at any 5, 12, or 15V signals within that one setting. In that fashion, we could look at an entire signal chain by just moving the scope probe and not adjusting the scope.

While troubleshooting, I heard a "pop" that sounded as if a circuit breaker or a polarized capacitor had exploded. I jumped back a few steps and then noticed the gaggle of engineers nearby who were trying to suppress their giggling. At my feet was the flexible cap of a plastic container—similar in size to the old 35-mm film canisters—that stored connector pins. The engineers had sprayed "freeze spray" into the container until the air and sides inside were at –50°C, then quickly capped the container and left it to sit at room temperature. After a few minutes, the air inside heated to room temperature, and the resultant pressure forced off the cap. Creative coworkers have always liked to "help" in difficult situations.

I rapidly moved the scope probe and looked at all the logic-level signals on the board's complement of ICs. At first glance, everything looked OK. I then went back and slowly examined each waveform. Instead of a large TTL-level voltage swing out of the 74LS04, I was getting a 2V swing. A closer look revealed logic levels of +5 and +3V dc. Even the ground pin was at 3V!

I carefully looked at the bottom of the board to examine the next IC in the signal path after the oscillator. Through the haystack of wires, I saw a wire on the V_{CC} (pin 14) going to +5V dc but did not see any wire on the ground (pin 7). The technician who had wired the boards made a habit of putting all the V_{CC} and ground connections on first. The other technician did not, however, and he had forgotten some of those ground connections. A quick wire wrap on each IC pin 7 to ground fixed the faulty boards.

So in this case of "haste makes waste," I learned that though a schematic can be absolutely correct and perfect, it takes an entire team to produce a successful product.EDN

Bruce Bushey, now a test engineer, was an electronics hobbyist for many years before starting electrical-engineering classes at North Dakota State University (Fargo, ND).

DANIEL VASCONCELLOS